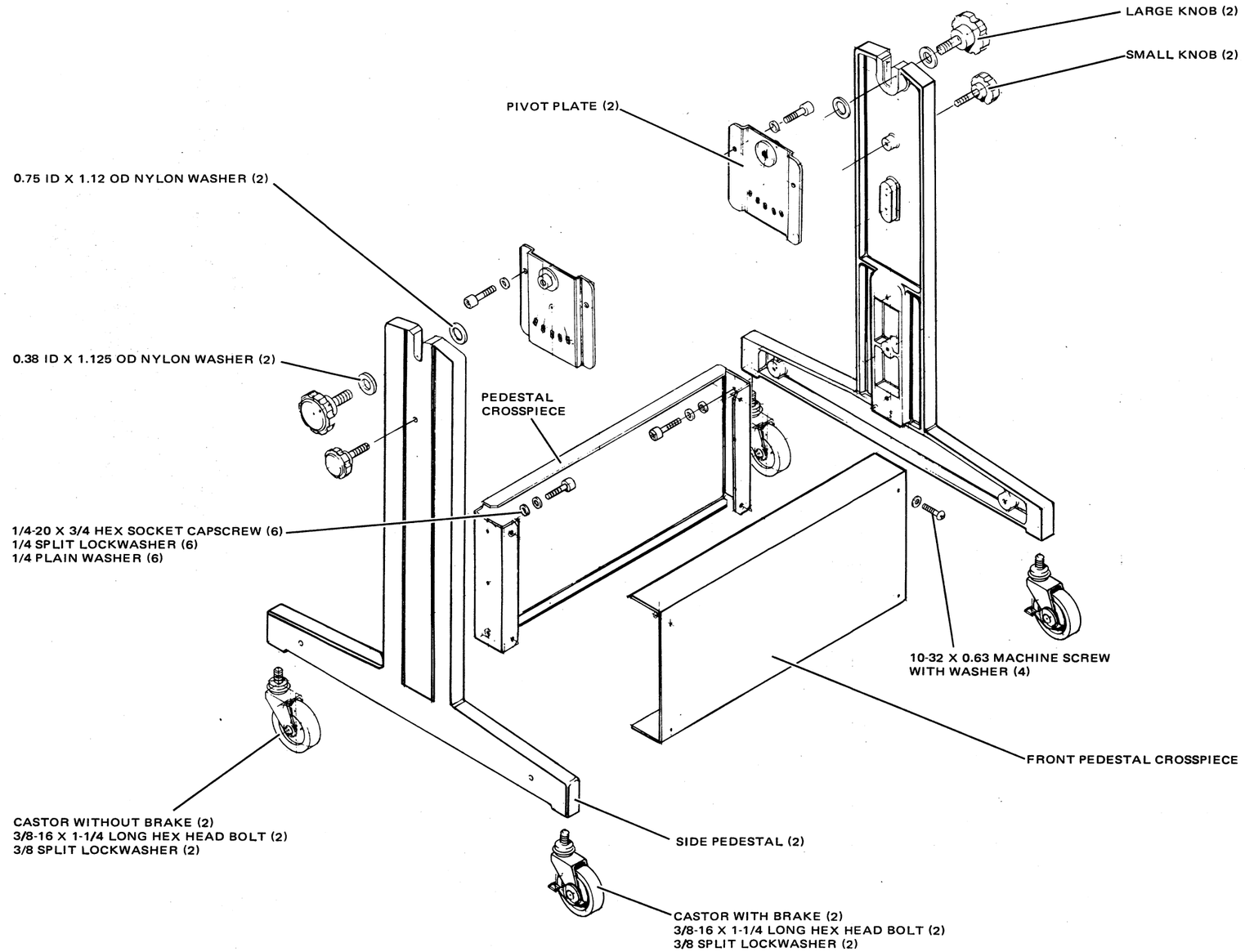


Figure 2-6.
Pedestal Assembly 4020485,
Exploded View

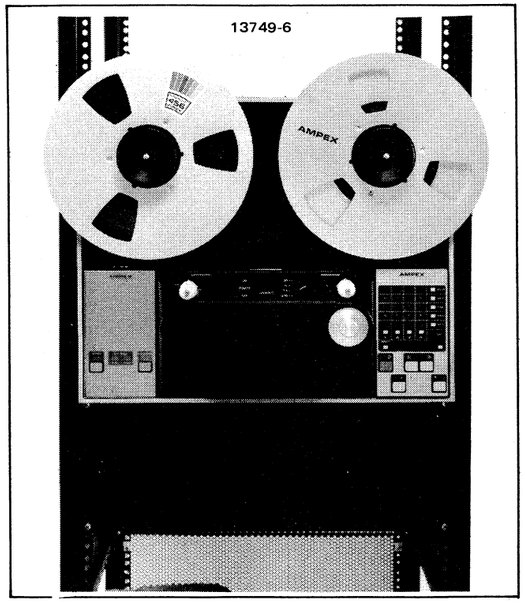


Figure 2-7. Rack Mount with Electronics Assembly (Front-Mounted)

captive power cable is attached to a power switch bracket mounted on the power supply (Figure 2-9). The main power transformer has various taps that permit the recorder/reproducer to use one of four input voltage ranges: 90-115, 110-135, 180-230, and 220-270 Vac, 50 or 60 Hz.

A jumper plug and socket arrangement (Figure 2-10) accessible inside the power supply, adapts the recorder/reproducer for the various input voltages. The jumpers are factory-set to 110-135 Vac unless specified otherwise on the sales order. However, the line voltage should be measured and, if required, the jumpers reset to correspond to the line voltage. Table 2-1 lists the various voltages and the corresponding jumper-plug position.

To change jumper plug positions, proceed as follows:

1. At the bottom side of the recorder/reproducer, loosen the four power supply cover screws and remove the cover to gain access to the power jumper socket (see Figure 2-10).

CAUTION

WHEN INSTALLING POWER JUMPERS, MAKE CERTAIN THAT THE 3-PIN POWER JUMPER DOES NOT MATE WITH PIN LOCATIONS 1, 2, OR 3 ON JUMPER SOCKET. ONLY THE 4-PIN POWER JUMPER MATES WITH PIN LOCATIONS 1, 2 OR 3.

2. Refer to Table 2-1 and install the three- and four-pin jumper plugs corresponding to the supplied ac line voltage. Note that both jumper plugs are installed vertically in column A, B, or C.

3. Replace power supply cover and secure with four screws.

2-14. AUDIO SIGNAL CONNECTIONS

The ATR-100 recorder/reproducer system comes equipped with an input/output assembly and usually the audio input and output connections are made to this assembly. However, for special operating or servicing purposes, information is also furnished in the following paragraphs for connecting the audio input and output signals directly to the recorder/reproducer.

All audio signal input and output connections to the basic recorder/reproducer are unbalanced line. All audio signal input and output connections to the input/output assembly can be either balanced or unbalanced line.

2-15. Recorder/Reproducer Input/Output Connectors

The audio signal input and output connectors (J13 and J14) on the recorder/reproducer are located at the bottom of the electronics assembly (Figure 2-11). All signal input and output connections for channels 1 and 2 are made to J13, and connections for channels 3 and 4 are made to J14. Use 24-pin Amphenol connectors (Ampex Part No. 139-840) furnished with the recorder/reproducer. Tables 2-2 and 2-3 provide a description

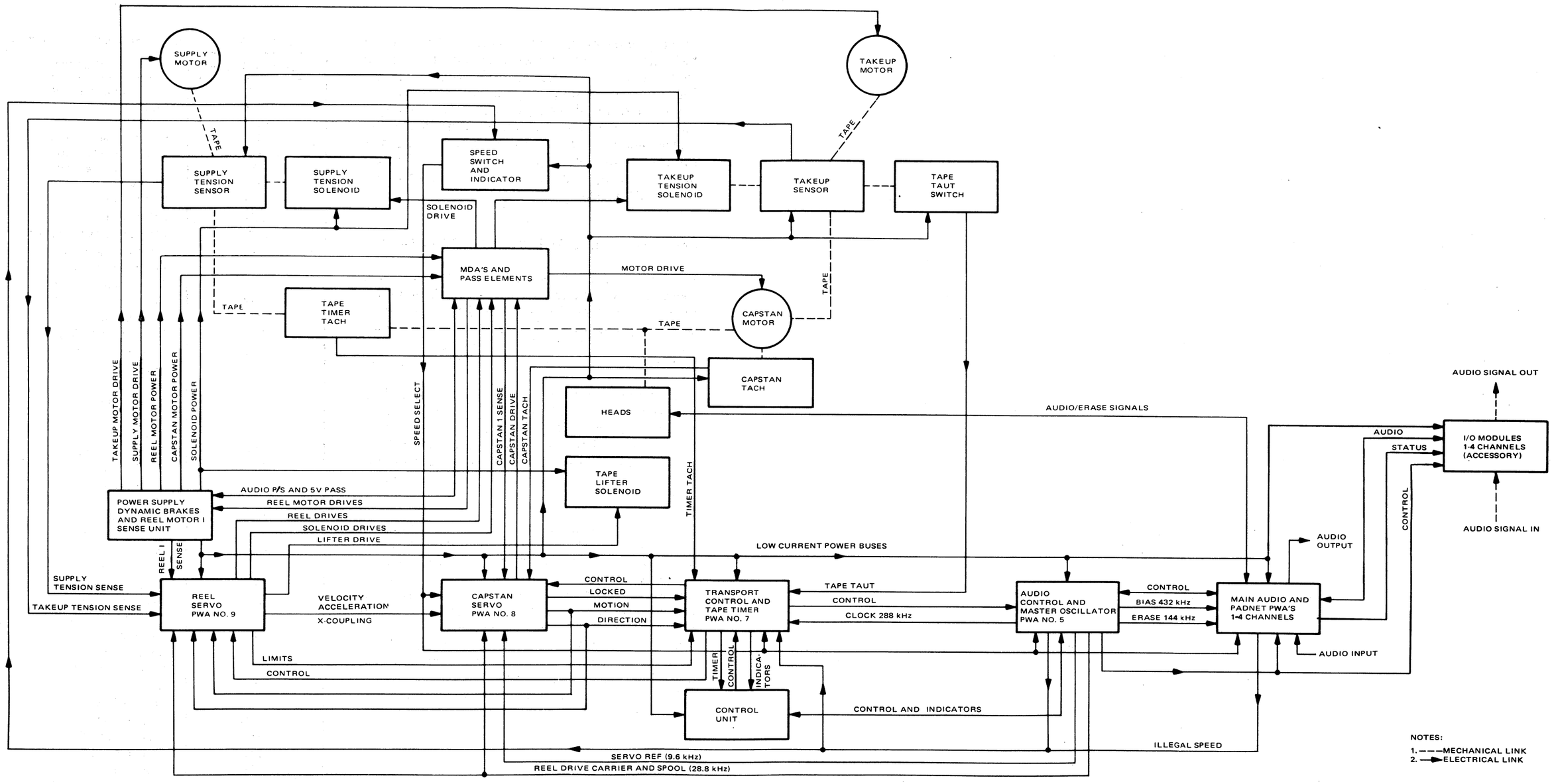


Figure 4-1. ATR-100 System, Simplified Block Diagram

display indicators. The transport tape timer tachometer furnishes pulses when tape is in motion to the tape timer circuitry on Transport Control PWA 7. Timer display information, in the form of a serial stream of binary-coded decimal digits, is sent to a decoder in the control unit. Digit select signals are also routed from Transport Control PWA 7 to the control unit in order to select the digit for display in the proper sequence on the tape timer LED display.

4-9. DETAILED THEORY OF OPERATION

Detailed theory of operation of the recorder/reproducer and input/output assembly is presented in the text that follows. Simplified functional block diagrams support the text as an aid in understanding the ATR-100 circuitry. For the complete schematic diagrams, see Section 6 of this manual.

Logic elements are identified in the text and block diagrams by their schematic reference designator and output pin number. For example, A3-1 refers to integrated circuit A3, output pin number 1. In the case where there is more than one output pin, the true (high) or active output pin designation is used.

Logic level commands used throughout the system are designated on the schematics and block diagrams by their three-letter abbreviation. All commands are a logic low, except for the LFT command and where complimentary logic is required. For example, the ready/safe command is so identified in the text but is designated $^{ready}\urcorner\llcorner_{safe}$ on the block diagrams. This indicates the ready command is a logic high and the safe command is a logic low. Table 4-1 is an alphabetical list (by abbreviation) of all commands used throughout the system.

Table 4-1. Command Signal Abbreviation

ABBREVIATION	COMMAND
BCD – A – D	Binary-coded decimal drive to 7-segment decoder

Table 4-1. Command Signal Abbreviation (Continued)

ABBREVIATION	COMMAND
BCS	Bias command status
BVS	Bias voltage status
CLK	Clock
CRB	Counter reset button
CS1 – 4	Channel select buttons
DRC	Command direction
DS1 – 5	Digit select lines
EDB	Edit button
EDI	Edit indicator
ERS	Electronics record status
EVS	Erase voltage status
FFB	Fast forward button
FFI	Fast forward indicator
ILM	Inner limit
IPB	Input button
ISL	Illegal speed lockout
LFT	Tape lift command
LKD	Locked
MRB	Main record bus
MTS	Motion sense
OLM	Outer limit
PDR	Play and record
PEC	Play edit command
PLB	Play button
PLC	Play command
PLI	Play indicator
RCB	Record button
RCI	Record indicator
RDB	Ready button
RED	Remote edit
RPB	Reproduce button
RWB	Rewind button
RWI	Rewind indicator
SFB	Safe button
SHC	Shuttle command
SPC	Spool command
SSA	Speed select A
SSB	Speed select B
STB	Stop button
STC	Stop command
STI	Stop indicator
STP	Stop pulse
SVO	Servos on command
SYB	Sync button
TDR	True direction
TLM	Torque limit
TTS	Tape taut switch
WUL	Wake-up line

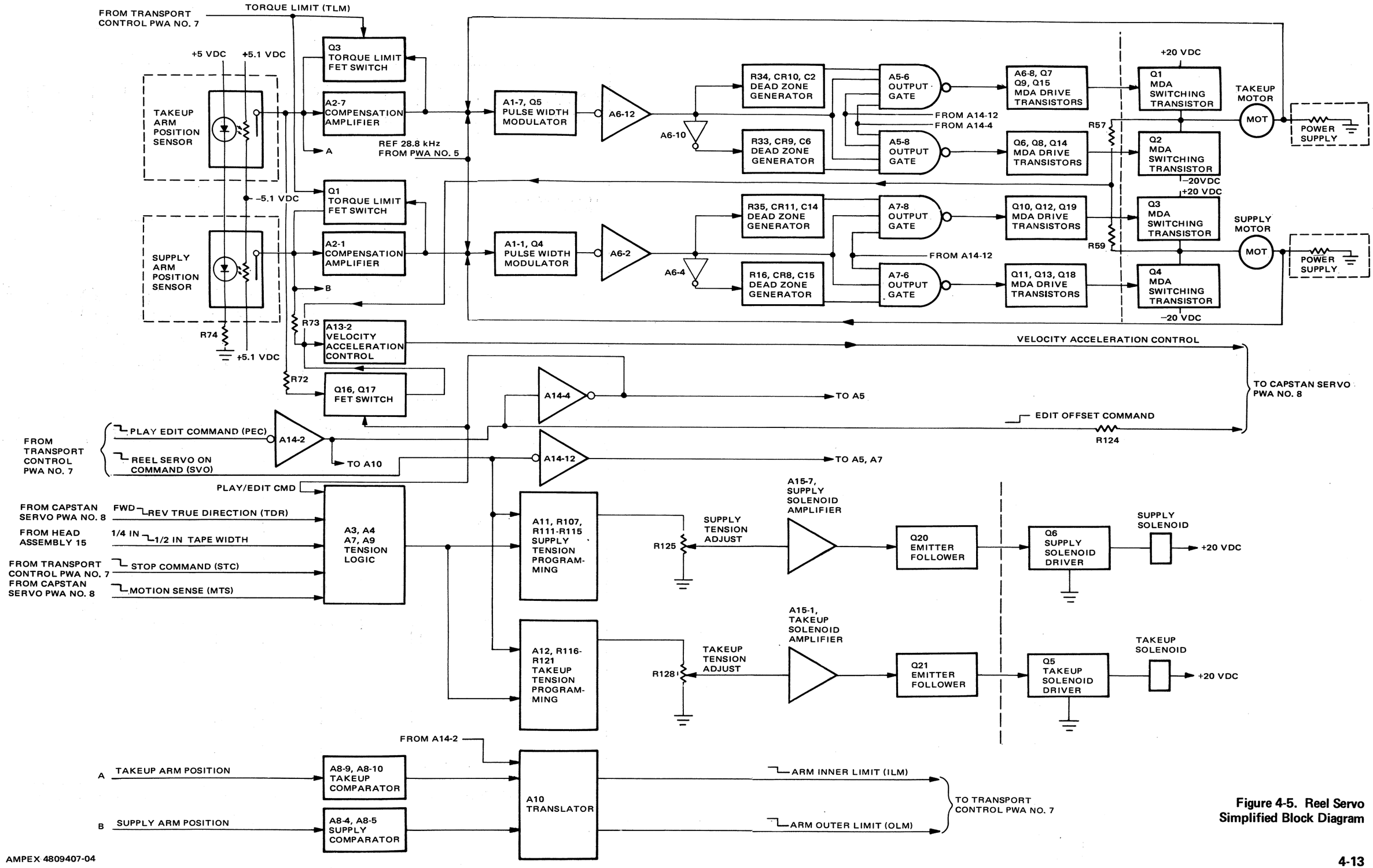


Figure 4-5. Reel Servo Simplified Block Diagram

AMPEX 4809407-04

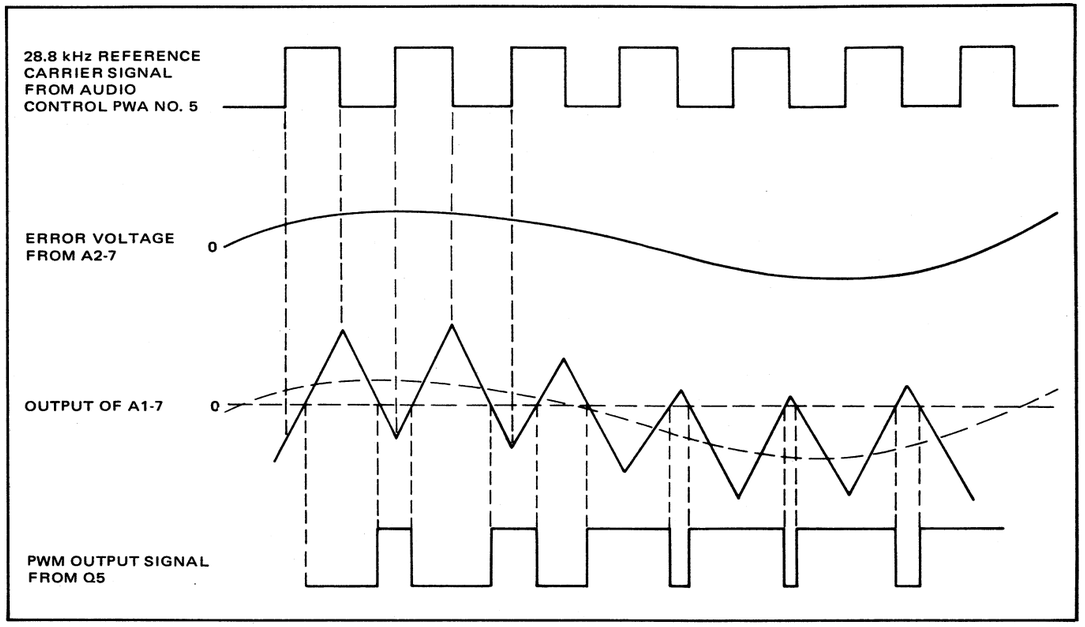


Figure 4-6. Pulse Width Modulator Waveforms, Takeup Reel Servo

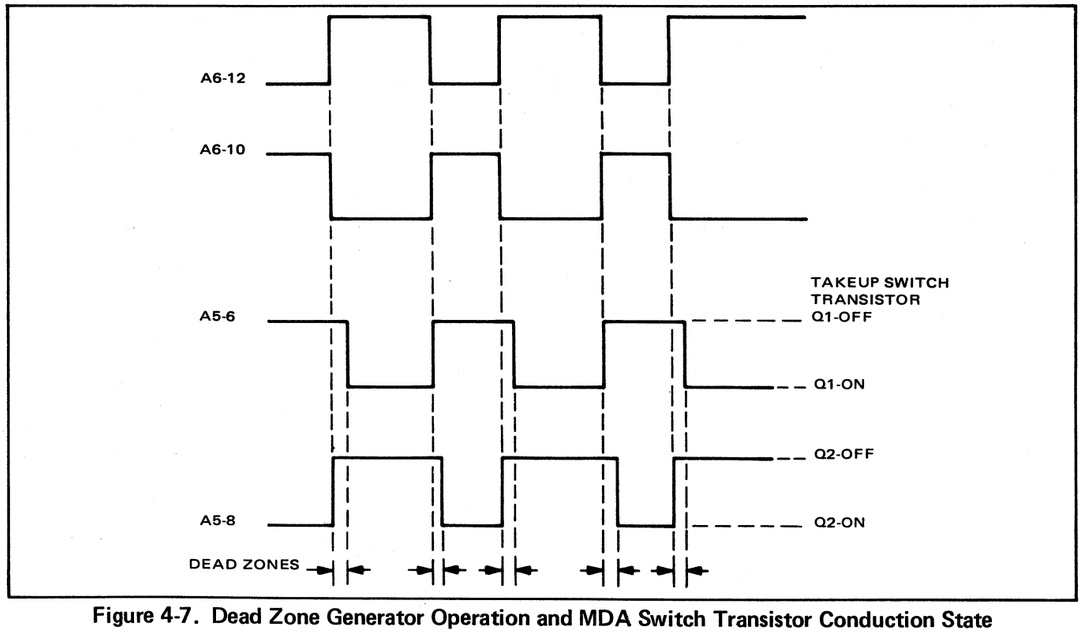


Figure 4-7. Dead Zone Generator Operation and MDA Switch Transistor Conduction State

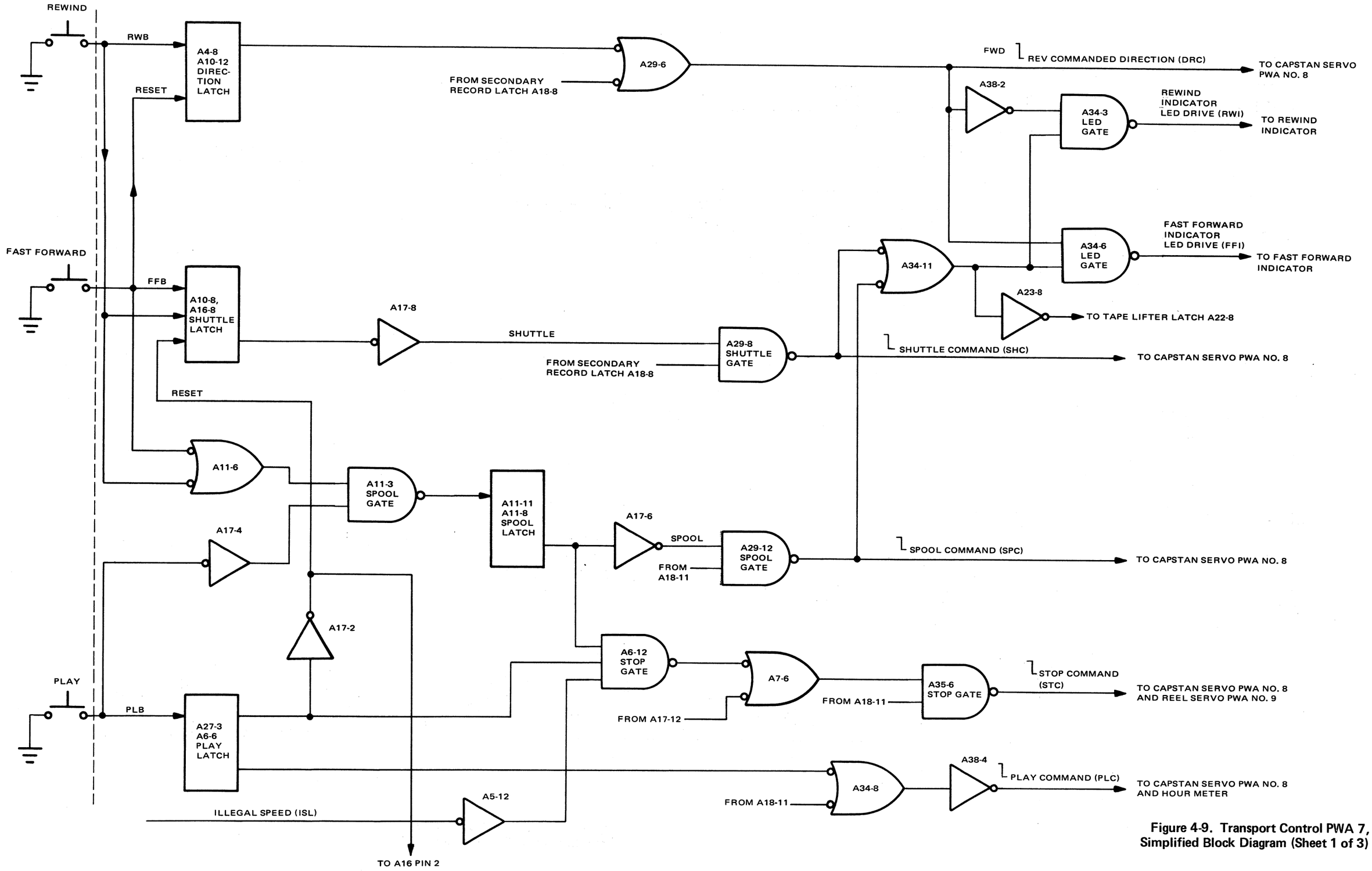


Figure 4-9. Transport Control PWA 7, Simplified Block Diagram (Sheet 1 of 3)

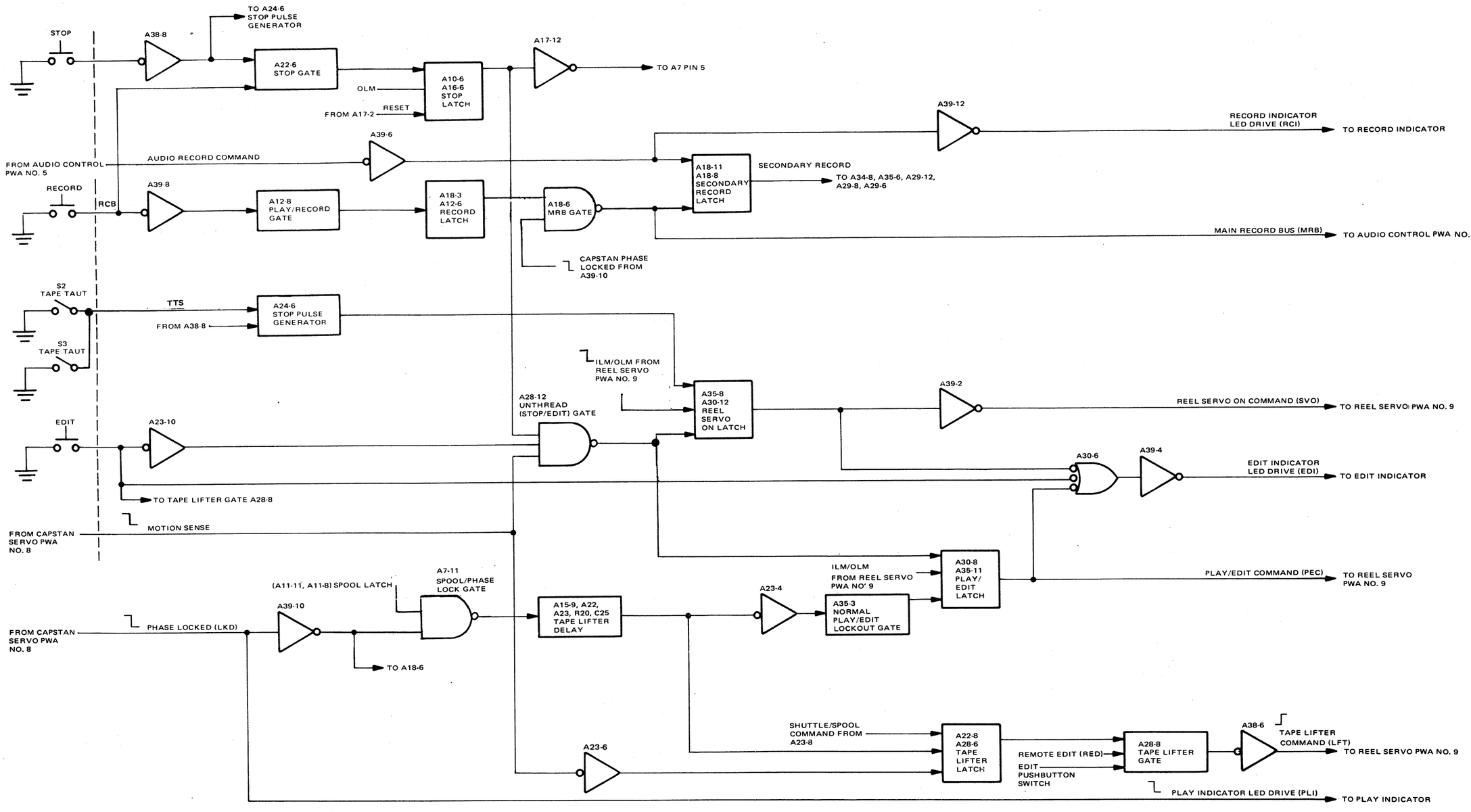


Figure 4-9. Transport Control PWA 7, Simplified Block Diagram (Sheet 2 of 3)

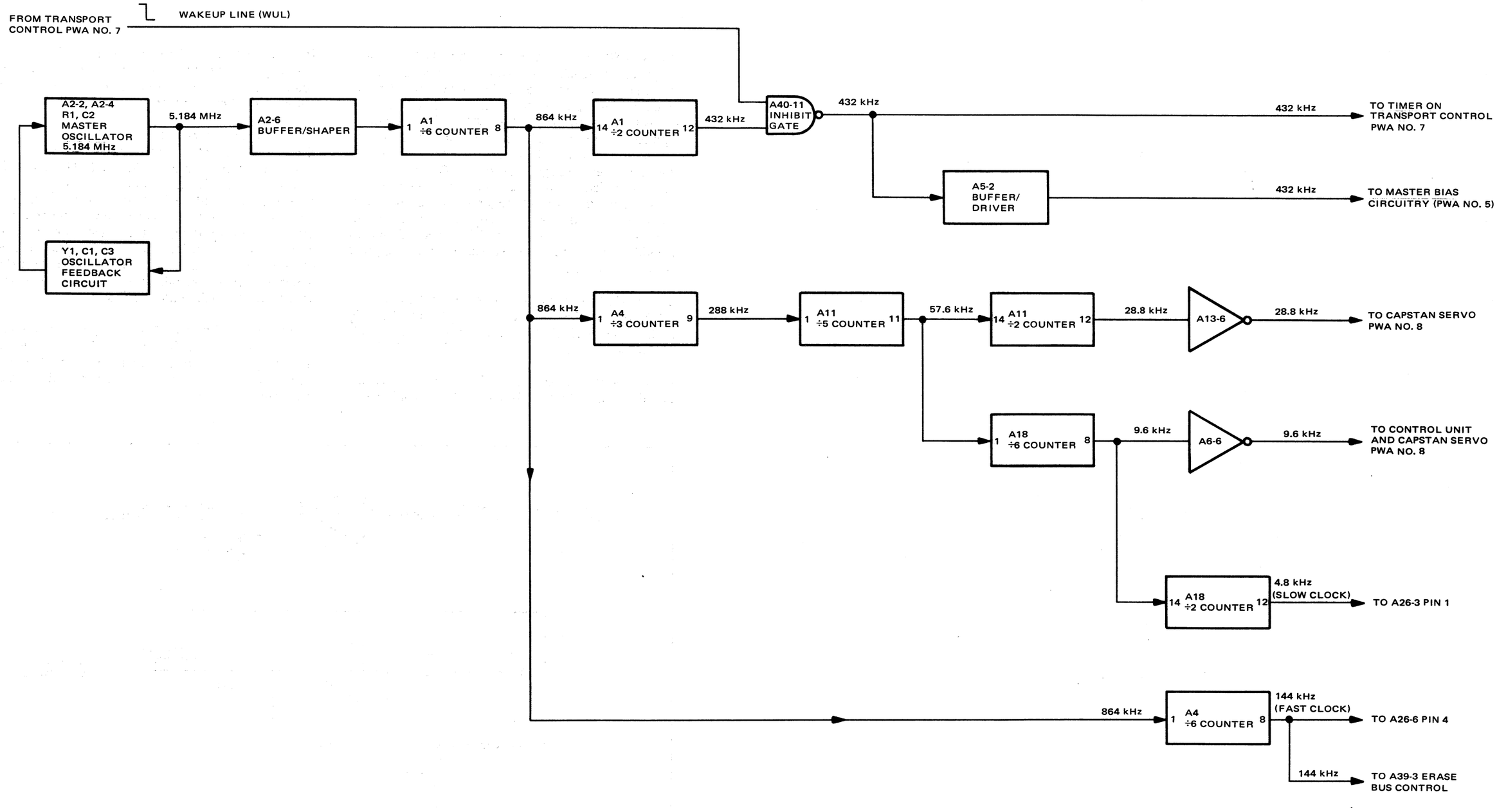


Figure 4-14. Master Oscillator and Counters, Simplified Block Diagram (PWA 5)

Resistor R1, in parallel with inverter A2-2, provides negative feedback and causes the inverter to try to operate as a linear amplifier. Any small disturbance at the input of A2-2 appears as an in-phase transition at the output of A2-4. This signal is applied to divider C1/C3, and the signal at the junction of C1 and C3 is fed back to the input of the amplifier through crystal Y1. Crystal Y1 acts as a very-high-Q tuned series-resonant circuit that passes only the desired frequency of 5.184 MHz. Capacitor C2 bypasses undesired harmonics and inverter A2-6 buffers the 4.184-MHz signal to provide a clean square-wave signal that is applied to the divider chain.

The 5.184-MHz signal is divided down by counters A1-8, A1-12, A4-8, A4-9, A5-2, A11-11, A11-12, A18-8, and A18-12 to provide the various signals shown on simplified block diagram Figure 4-14.

4-63. Master Erase Bus. The master erase bus circuitry accepts the 144-kHz TTL level signal from the master-oscillator counter and buffers the signal, lengthens the rise time, and provides an adjustable erase signal level that can be verified between the limits of 0 to 12 volts p-p.

As shown in Figure 4-15, the 144-kHz TTL level signal from counter A4-8 is fed through R33 to inverting CMOS amplifier A39-5/1. This amplifier serves as a buffer and ground translator which transfers the 144-kHz TTL level signal from logic ground to the audio system ground. The amplifier provides an output signal that swings between the limits of 0 and +5 Vdc. This output signal is applied across the master erase bus level control R34 which is used to establish the erase bus signal level applied to the main audio PWA's.

In the event that the 15-Vdc operating voltage, applied to the CMOS device A39, should be removed while an input signal is present, R33 will limit the input current and prevent the device from being damaged.

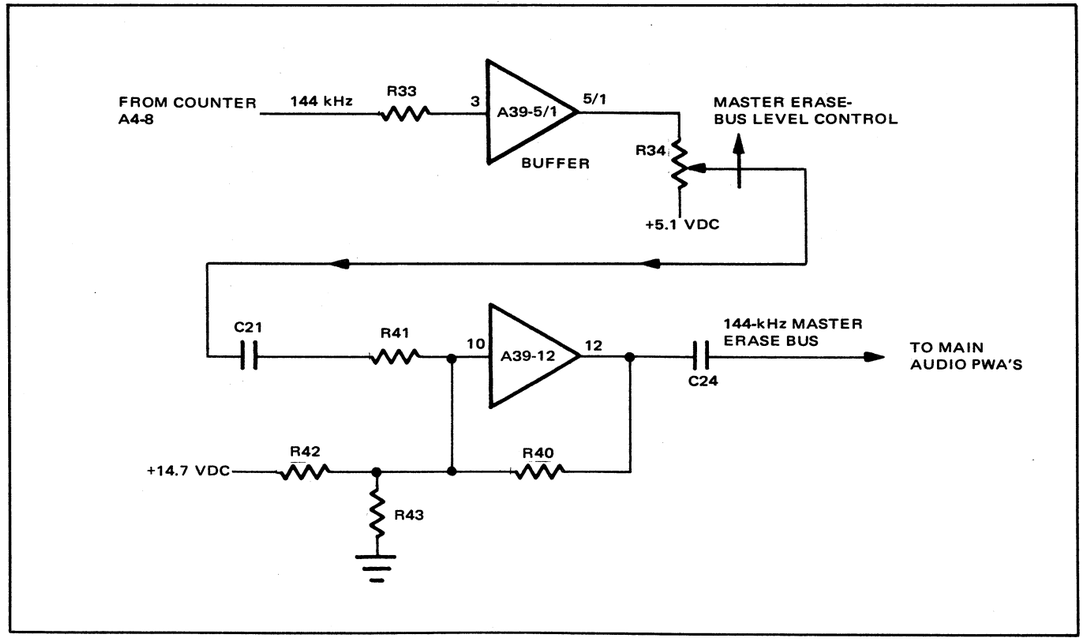
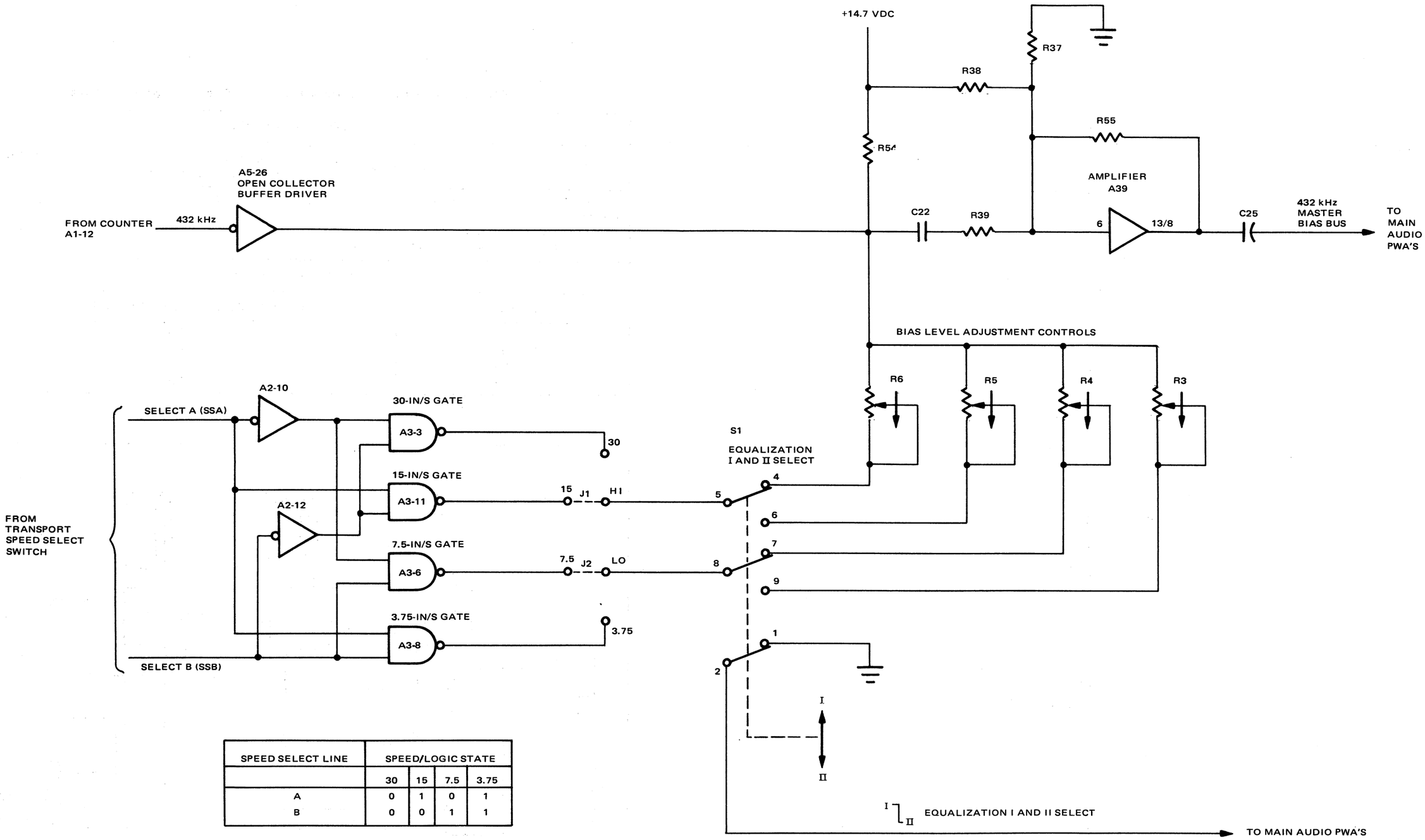


Figure 4-15. Master Erase Bus, Simplified Schematic Diagram, Audio Control PWA 5



SPEED SELECT LINE	SPEED/LOGIC STATE			
	30	15	7.5	3.75
A	0	1	0	1
B	0	0	1	1

Figure 4-16. Master Bias Bus, Two-Speed Simplified Schematic (PWA 5)

Table 4-6. Speed Jumper Placement and Bias Switch Setting, Audio Control PWA 5

2-SPEED OPERATION			
SPEED	**SET JUMPERS TO DESIRED SPEED**	**MASTER BIAS (ADJUST S1 POSITION I)**	**MASTER BIAS (ADJUST S1 POSITION II)**
HI SPEED LO SPEED	J1 – 30, 15, 7.5 J2 – 15, 7.5, 3.75	R6 R4	R5 R3
NOTE: J3 and J4 to be jumpered to the S (store) positions.			

4-SPEED OPERATION	
JUMPER	**MASTER BIAS (ADJUST S1 POSITION I ONLY)**
J1 – 30 J3 – 15 J2 – 7.5 J4 – 3.75	R6 R5 R4 R3

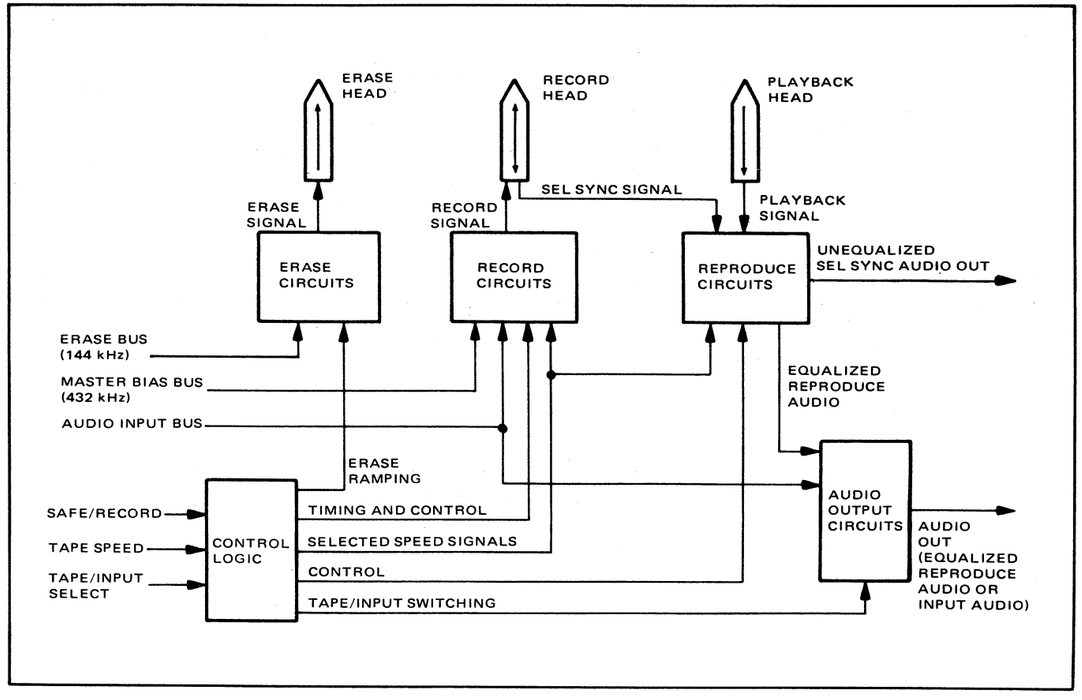


Figure 4-17. Main Audio Simplified Block Diagram

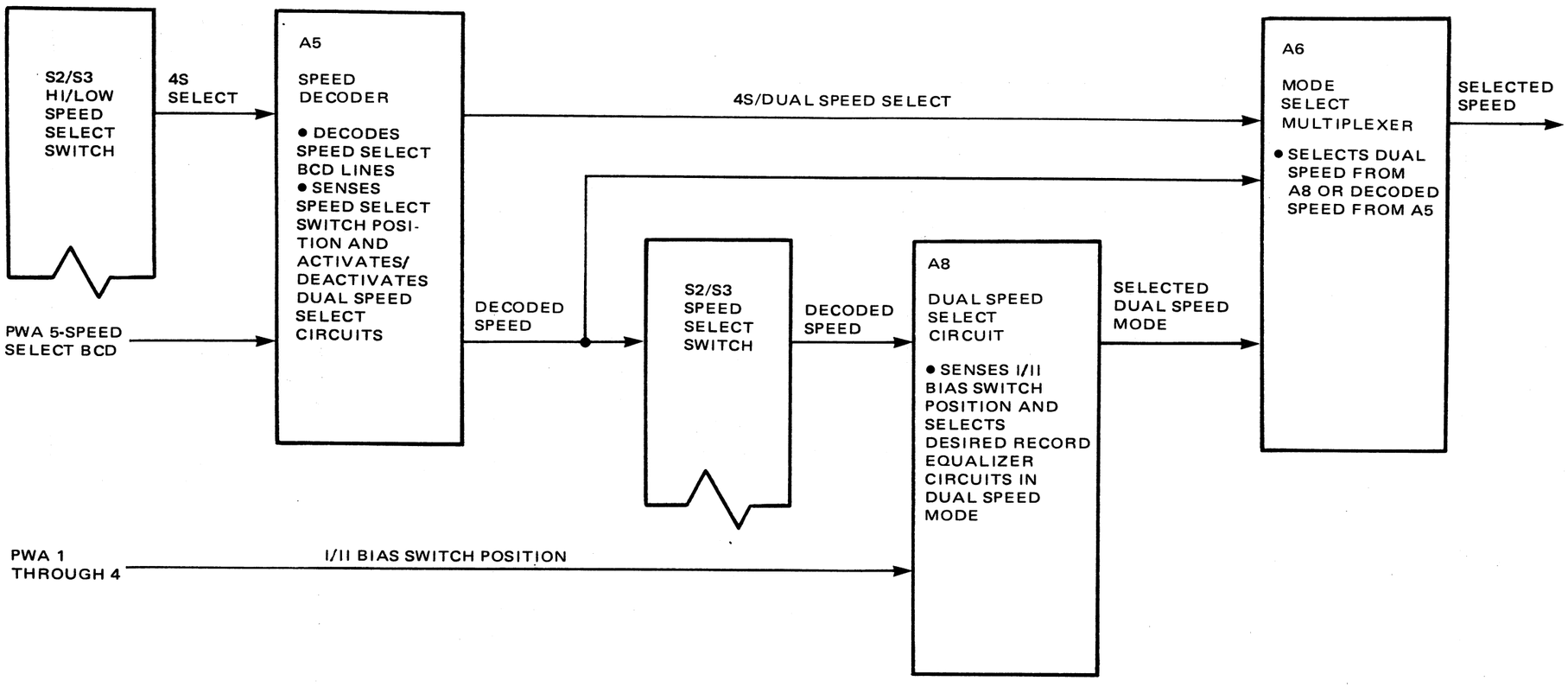


Figure 4-25. 4-Speed PADNET
Tape Speed Circuits,
Simplified Block Diagram

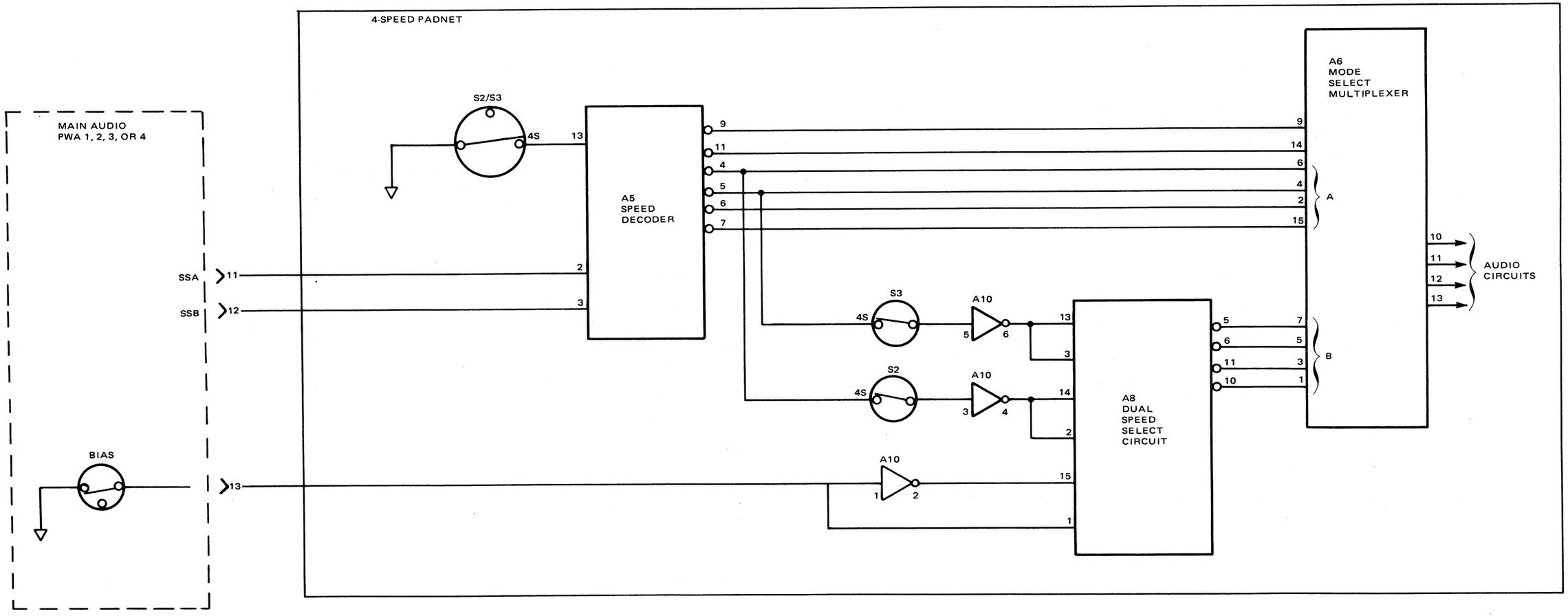
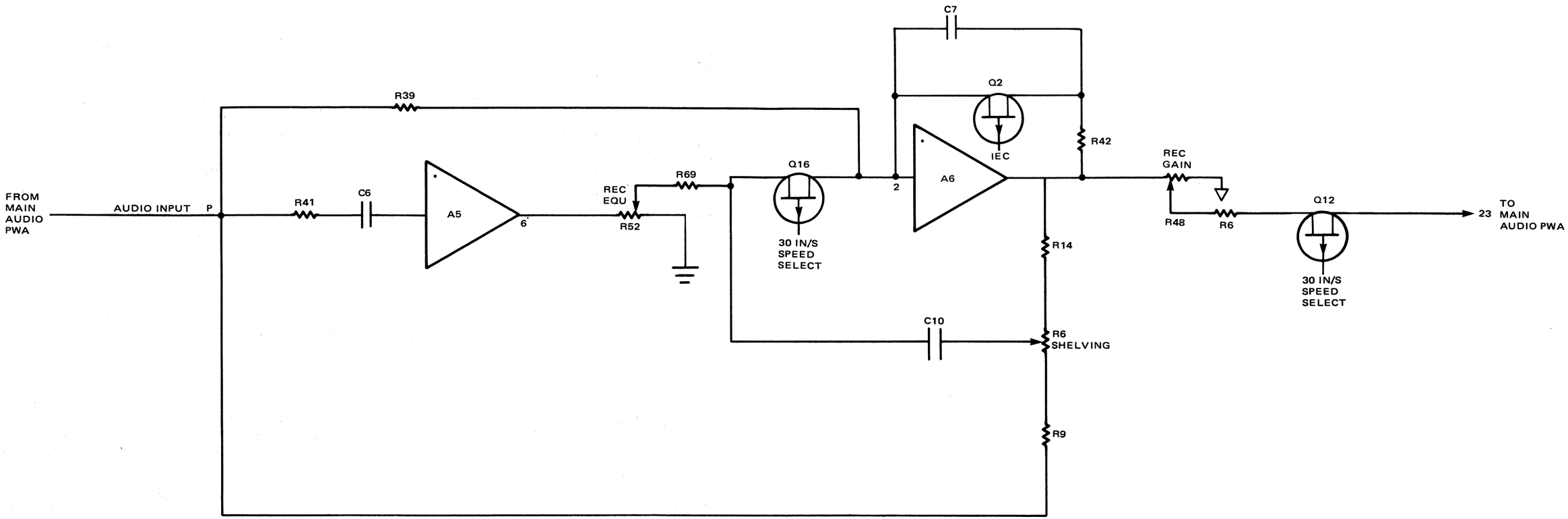


Figure 4-26. 4-Speed PADNET Tape Speed Select Circuits, Simplified Block Diagram



*LOCATED ON MAIN AUDIO PWA

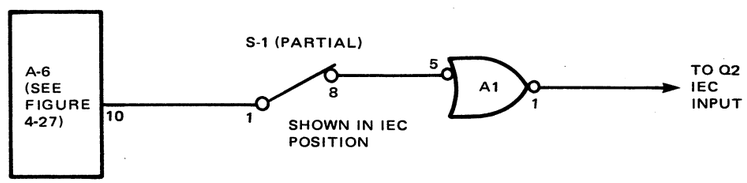


Figure 4-30. Simplified Schematic Record Circuits 30 in/s Tape Speed 4S Only

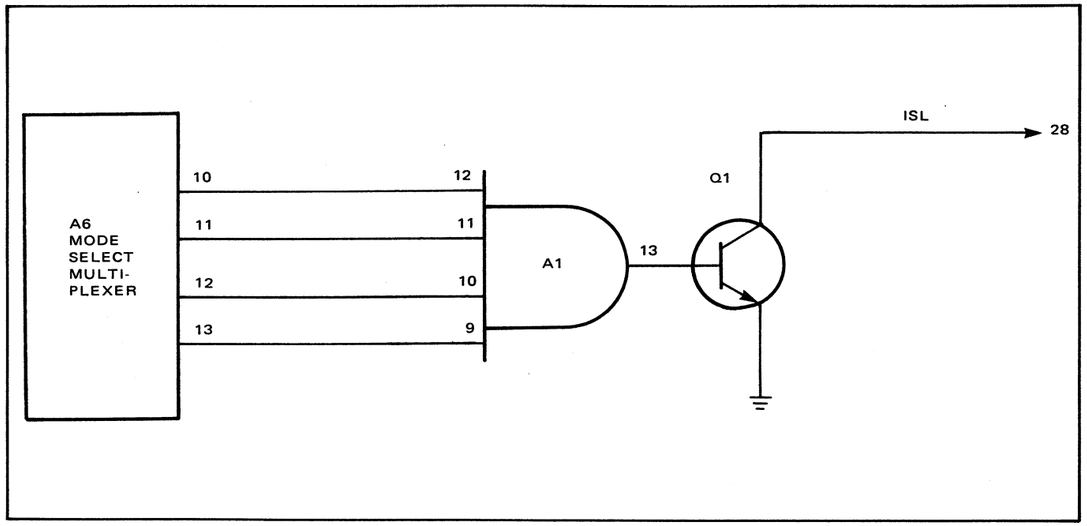


Figure 4-31. Illegal Speed Signal Generator, Simplified Schematic

capacitor C7 is shorted out by FET switch Q2. When 4S is selected and the 30 in/s is activated, the low on pin 1 of S1 is felt on pin 8 when the first portion of S1 is in the ON position. This low is routed to OR gate A1. The low on pin 1 of A1 activates FET switch Q2 shorting out C7. The path, for any other tape speed with the appropriate portion of S1 closed, will be similar.

4-84. Illegal Speed Signal Generator. (See Figure 4-31). An illegal speed signal (ISL) is generated when a speed is selected on the speed select rotary switch that the S2/S3 speed select switches on the PADNET are not configured to accommodate or if S2 and S3 are both set for the same speed.

When an illegal speed is selected all the outputs of mode select multiplexer A6 go high, enabling AND gate A1. The high on pin 13 of A1 turns Q1 on and the ground on the emitter of Q1 is routed to pin 28 of the PADNET. When S2 or S3 on the PADNET is in the 4S position, a wrong speed signal cannot be generated.

4-85. Bias Normalizing and Filtering Circuits (See drawing No. 4840468). The 432-kHz bias signal enters the PADNET on pin FF where it is routed to the bias normalizing and filtering circuits. Bias normalizing resistor R1/R2 provides level setting of the received 432 kHz from the master bias bus via BIAS NORM potentiometer R1. The level normalized bias signal is then filtered by bandpass filter L1/C1 on the PADNET. The bias signal is then routed to pin 26 on the PADNET and pin 26 on the main audio boards.

4-86. Input/Output Assembly

Up to two input/output modules may be mounted side-by-side in an input/output assembly. One module is required for each audio channel, and each module contains a line input and a line output transformer that permits balanced line operation, a line driver, switchable peak/vu level meter, and input and output level controls with preset/manual switch controls. Figure 4-32 is a simplified block diagram of the input/output assembly, drawing 4840427 is the schematic of the input/output mainframe assembly, and drawing 4840421 is the schematic of the input/output module (schematics are in Section 6 of this manual).

4-87. Line Input Amplifier. The audio line input signal to be recorded is applied to the input of

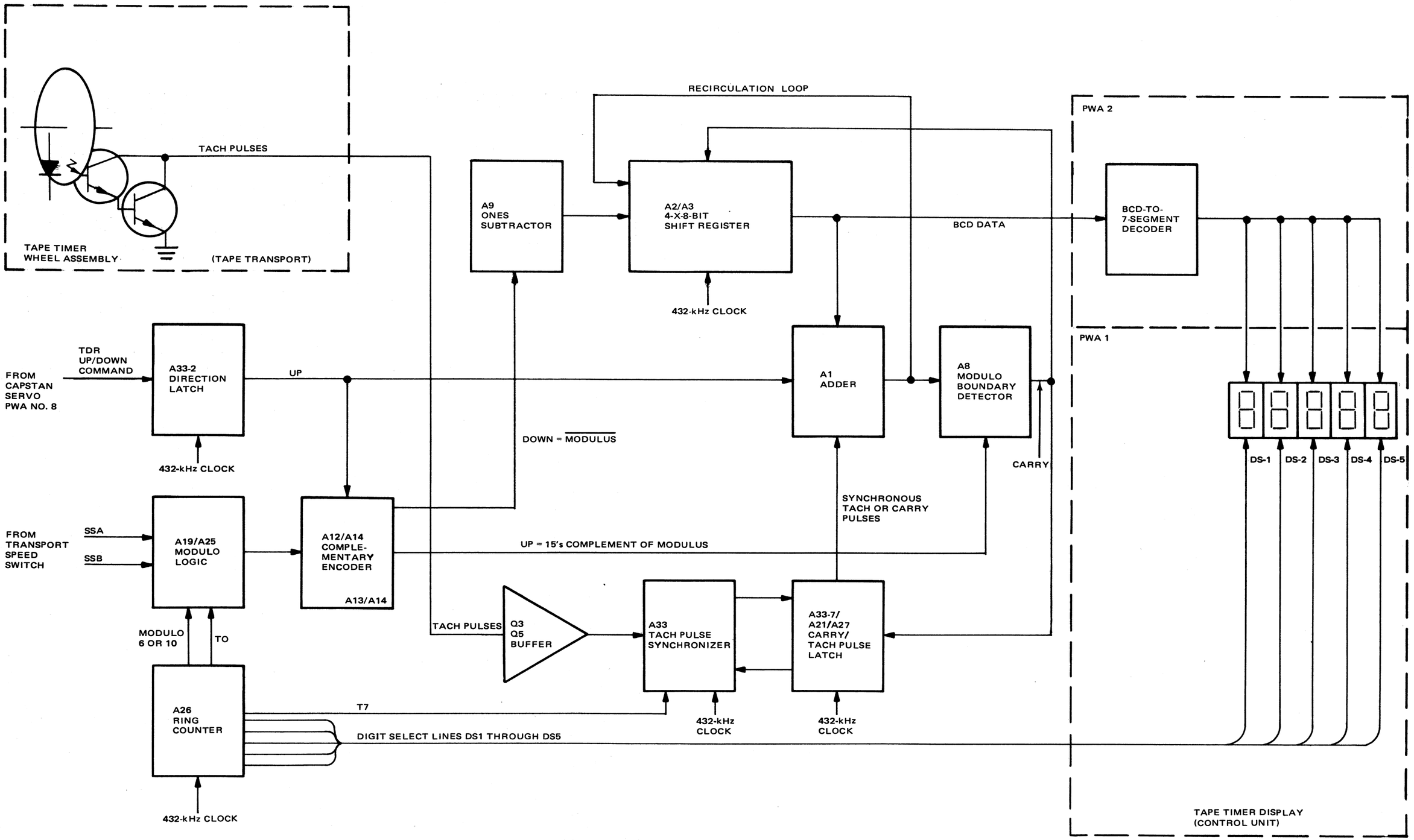


Figure 4-33. Tape Timer, Simplified Block Diagram

Table 4-8. Counter Data Word Format

MODULO	TIME
Tape-Speed Divider (modulo depends on tape speed selected)	t_0
Tenths of Seconds (modulo 10)	t_1
Units of Seconds (modulo 10)	t_2
Tens of Seconds (modulo 6)	t_3
Units of Minutes (modulo 10)	t_4
Tens of Minutes (modulo 6)	t_5
Units of Hours (modulo 10)	t_6
Tens of Hours (modulo 10)	t_7

speed. Since the tach pulses are generated at a rate of 20 times per 7.5 inches of tape, the modulus of the digit at time t_0 varies with the tape speed selected to divide the tach pulses by a factor which provides 10 pulses per second at the selected operating speed. At a selected operating speed of 30, 15, 7.5, and 3.75 inches per second, the modulus of the digit at t_0 is 8, 4, 2, and 1, respectively. The digits at times t_1 through t_7 represent the operating time in hours, minutes, seconds, and tenths of a second at the selected operating time. Only five digits are displayed on the control unit.

The digits at time t_1 through t_5 or at time t_2 through t_6 may be selected by link strapping on the tape timer logic assembly to display tenths of a second, seconds, and minutes or to display seconds, minutes, and hours, respectively, on the control unit display. The output signals from the ring counter are strapped to the enable signal lines, DS-1 through DS-5, to select the appropriate digit on the control unit display.

The tape up/down counter in the tape timer logic consists of shift register A2/A3, adder A1, ones subtractor A9 modulo boundary detector A8, and carry flip-flop A33-7. The up/down counter shifts each digit in the counter data word in a 4-bit slice to the data output lines. If a tach pulse is not received by the tape timer logic within the previous cycle (t_0 through t_7), the data is recirculated through the up/down counter without being modified. If a tach pulse is received by the tape timer logic during the previous cycle (t_0 through t_7), the count in the up/down counter is incremented by one when the tape motion is in a forward direction, or decremented by one when the tape motion is in the reverse direction.

The timing and control logic of the tape timer consists of ring counter A26, direction latch A33-2, modulo logic A19/A25, complementary encoder A13/A14, and tach pulse latch A21/A27. Ring counter A26 is clocked by the positive-going edge of the 432-kHz signal and generates the 8-bit time intervals (t_0 to t_7) for one cycle of operation of the up/down counter. The modulo logic A19/A25 receives the speed selector signals, SSA and SSB, from the tape transport speed selector switch and timing information from the ring counter A26. The modulo logic generates the 15's complement of the modulus for each digit in the counter data word at the corresponding time interval. The modulo information, in 15's complement form, is sent to complementary encoder A13/A14. Complementary encoder A13/A14 provides the modulus or its complement to ones subtractor A9 or modulo boundary detector A8, respectively. Direction latch A33-2, which is set by the tape up/down command TDR, generates the control signal UP to complementary encoder A13/A14. The UP signal, if set (high), gates the complemented modulus to modulo boundary detector A8. If the UP signal is reset (low), the modulus is sent to subtractor A9. The UP signal is also sent to adder A1 where it provides the control signal to increment to decrement the counter when a tach pulse has been received.

The modulo information is sent to the complementary encoder A13/A14 which provides the modulus or its complement to the ones subtractor A9 or the modulo boundary detector A8, respectively. Tape direction latch A33-2, which is set by the tape up/down command (TDR), generates the control signal (UP) to the complementary encoder A13/A14. The UP signal, if set (high), gates the 4-bit complement of the modulus to modulo boundary detector A8. If the UP signal is reset (low), the modulus is sent to the ones subtractor A9 in BCD. The UP signal is also sent to adder A1 where it provides the control signal to increment or decrement the counter when a tach pulse has been received.

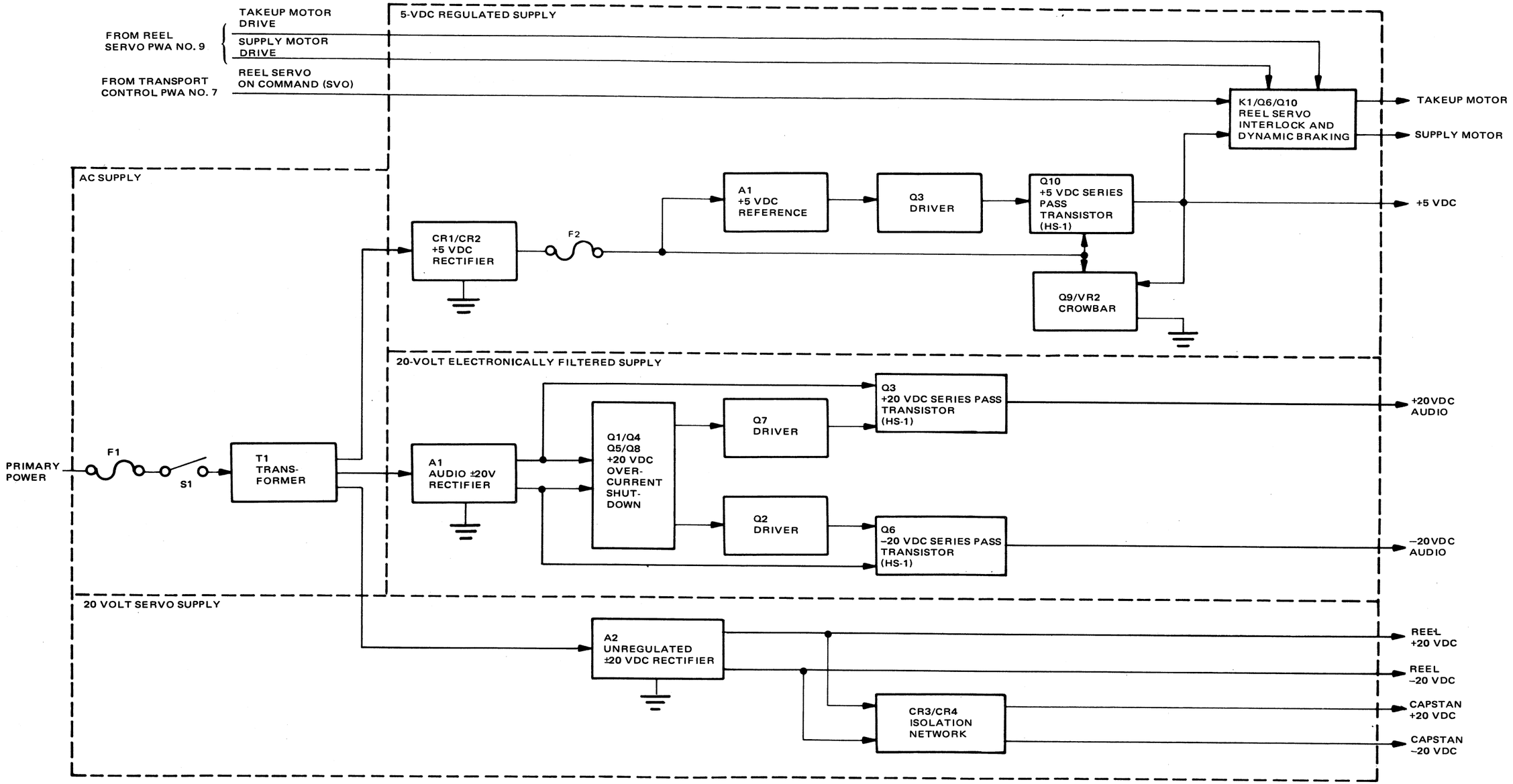


Figure 4-36. Power Supply Assembly, Simplified Block Diagram

capacitor C7, –20-Vdc floating reference capacitor C3, overcurrent shutdown transistors Q5/Q8/Q4/Q1, +20-Vdc driver Q7, –20-Vdc driver Q2, +20-Vdc series-pass transistor Q8, and –20 Vdc series-pass transistor Q9. (Q8 and Q9 are located on the transport heat sink.) The 20-volt electronically filtered supply provides +20 Vdc and –20 Vdc (22 Vdc, nominal) for use by the audio circuits. The 20-volt rectifier A1 is a bridge rectifier assembly connected to the secondary winding of transformer T1 to act as two full-wave rectifiers; one rectifier to provide the +20 Vdc and the other rectifier to provide the –20 Vdc. The outputs of 20-volt rectifier A1 provide the +20-Vdc and –20-Vdc floating references via capacitor C7 and driver Q7 for the +20-Vdc and via capacitor C3 and driver Q2 for the –20 Vdc. Drivers Q7 and Q2 provide the electronically filtered +20 Vdc and –20 Vdc to the +20-Vdc series-pass transistor Q8 and –20-Vdc series-pass transistor Q9, respectively. Overcurrent shutdown transistors Q5/Q8/Q4/Q1 provide dual shutdown of the +20-Vdc and –20-Vdc outputs when excessive current is drawn from either output. If excessive current is drawn from either +20-Vdc or –20-Vdc output, overcurrent shutdown transistors Q5/Q8/Q4/Q1 will cause both outputs to go to 0 Vdc and remain at 0 Vdc until power is removed for approximately 10 seconds and reapplied. Transistors Q5 and Q4 and resistors R6 and R16 provide current sensing for the +20-Vdc and –20-Vdc outputs, respectively. The output at the collectors of Q5 and Q4 go to the bases of each other and to the bases of transistors Q8 and Q1, which shunt the floating references to drivers Q7 and Q2 and cause the outputs to go to 0 Vdc for both +20 Vdc and –20 Vdc.

4-107. 5-Vdc Regulated Supply. The 5-Vdc regulated supply consists of +5-Vdc rectifier CR1/CR2, +5-Vdc reference A1, +5-Vdc driver Q3, +5-Vdc series-pass transistor Q10, and crowbar Q9. The current for A1 is supplied from the audio +20V source. It is routed through R5, CR5, and filtered by C1. Additionally, reel servo interlock and dynamic brake K1/Q6/Q10 are operated from the 5-Vdc regulated supply. The 5-Vdc regulated supply provides the +5 Vdc to the TTL circuits on the ATR-100. The reel servo interlock and dynamic braking provides dynamic braking of the takeup and supply motors in the event of power failure or loss of reel servo control.

The +5-Vdc rectifier CR1/CR2 consists of a full-wave rectifier and associated filter capacitor. The rectified +5 Vdc goes to +5-Vdc reference A1 and +5-Vdc series-pass transistor Q10, via a 5 ampere fuse (F2). The +5-Vdc reference A1 provides a reference voltage to the base of driver Q3, which is connected to +5-Vdc series-pass transistor Q10 in a darlington configuration. Series-pass transistor Q10 provides the current required by the TTL circuits at the reference voltage minus the voltage drop across the base-to-emitter drop of Q3 and Q10. Part of output from +5-Vdc series-pass transistor Q10 is sampled by crowbar Q9 via 5.6V zener diode VR2. When the voltage at the output of series-pass transistor Q10 rises above +5.6V plus the trip voltage required to trigger SCR Q9, the current through zener diode VR2 rises and provides the gate current to SCR Q9 in crowbar Q9/VR2. SCR Q9 is connected across the +5-Vdc input, to series-pass transistor Q10, and ground. When SCR Q9 conducts, the +5-Vdc input to series-pass transistor Q10 is shunted to ground causing fuse F2 to open.

Reel servo interlock and dynamic brake K1/Q6/Q10 contains relay driver Q6/Q10, double-pole double-throw relay K1, full-wave rectifier CR9/CR10, and motor loads DS1/R15 and DS2/R4. Reel servo interlock and dynamic brake K1/Q6/Q10 disconnects the output of supply motor MDA and takeup motor MDA from the supply and takeup motors, respectively, and connects the motor loads to the motor to provide dynamic braking when reel servo on (SVO) goes high or +5 Vdc is lost.

Full-wave rectifier CR9/CR10 provides +24 Vdc from transformer T1 to the high (A) side of relay coil K1. The return for relay coil K1 is provided by relay driver Q6/Q10. When SVO is low (0 Vdc) and +5 Vdc is present at the output of the 5-Vdc regulated supply, relay driver Q6/Q10 provides a return path and energizes relay coil K1. When K1 is energized, the supply motor MDA is connected to the supply motor and the takeup motor MDA is connected to the takeup motor. If SVO goes high or +5 Vdc is lost, K1 is de-energized. When K1 is de-energized, the takeup motor is switched from the takeup motor MDA to motor load DS1/R15 and the supply motor is switched from the supply motor MDA to motor load DS2/R4. Motor loads

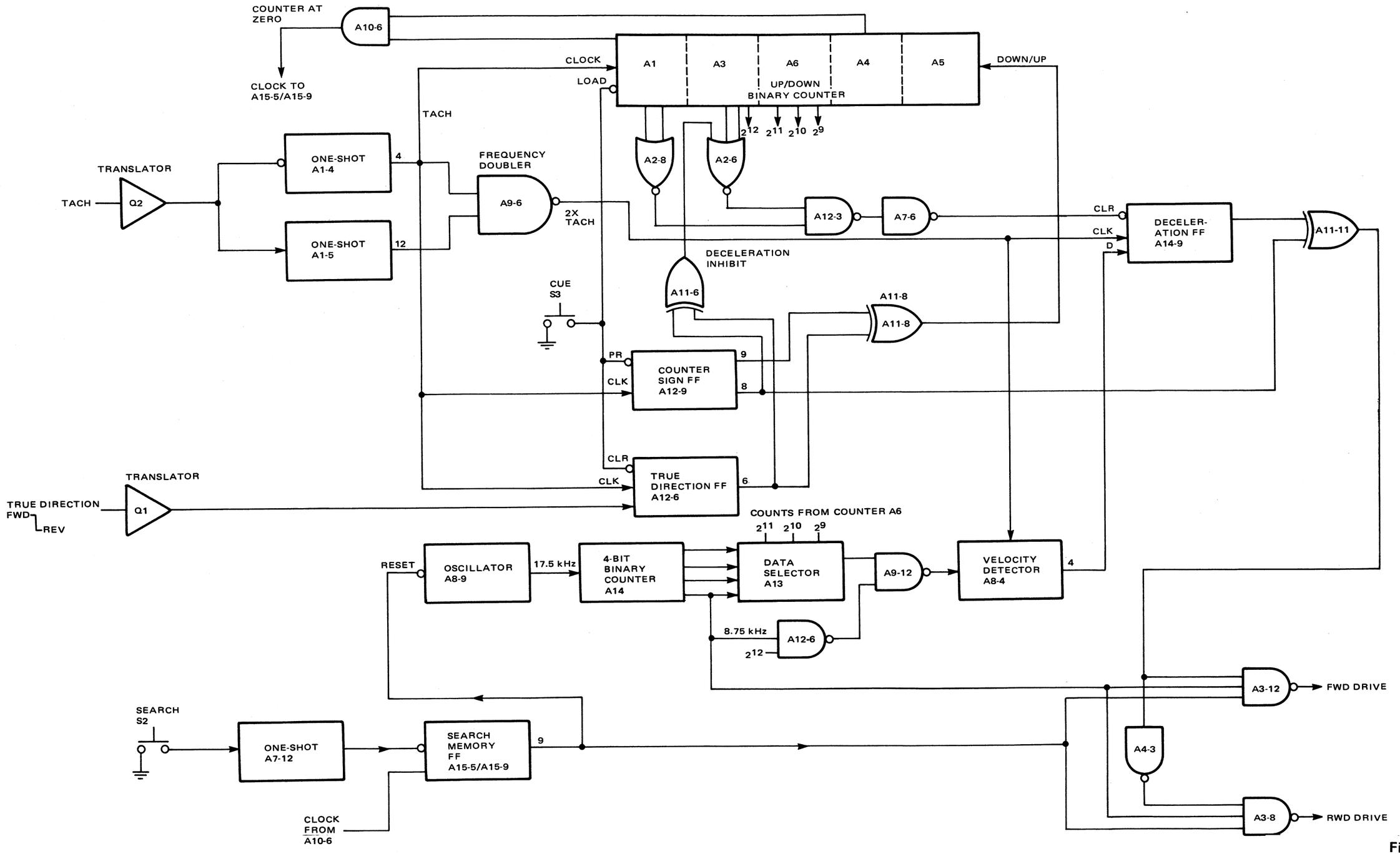


Figure 4-37.
Single-Point Search-to-Cue
Simplified Block Diagram

The high from A15-8 causes the SEARCH indicator light to go out. (Also wakeup circuit C9/R10 clears flip-flops A15-5/A15-9.) The high from A15-8 triggers one-shots A2-5 and A2-4. The low from A2-4 is inverted by A4-11 and A5-3 to supply a stop pulse, at pin 12 of the PWA, which is routed to the tape transport.

4-111. Search-Play Mode. If while in search mode the transport play pushbutton is pressed, the transport will enter play mode when the cue point is reached. In order to enter play mode, the SPSTC circuitry generates a play pulse with a longer duration than a stop pulse. While in search mode, the high from A15-9 enables 2.0 Hz oscillator A8-5, and pin 10 of gate A4-8 is enabled. When the transport play pushbutton is pressed, a low play command enters the PWA at pin 16 and is inverted by gate A4-6 and A4-8. The low from A4-8 presets play memory flip-flop A10-9. The high from A10-9 enables gate A9-11 which causes the PLAY indicator to flash at a 2 Hz rate. When the cue point is reached, counter PWA gate A10-6 is enabled as a result of counter A1, A3, A4, and A6 max/min output going high. This causes search memory flip-flops A15-5/A15-9 to be clocked low. The low from A15-9 causes FWD and RWD drive gates A3-12 and A3-8 to be inhibited, and the 2.0 kHz oscillator to be reset. The high from A15-8 triggers one shots A2-4 and A2-5, and the low going pulse from A2-4 is inverted by A4-11 and A5-3 to provide a low stop pulse. In order to then enter play mode, a train of play pulses is generated for a longer duration than the stop pulses. The high going pulse from play one-shot A2-5 enables gate A3-6 at pin 5 to pass the reference frequency from counter PWA A14-9 to generate a train of pulses for the play command. When A2-5 times out, the positive going trailing edge of the pulse from A2-12 resets the play memory flip-flop A10-9.

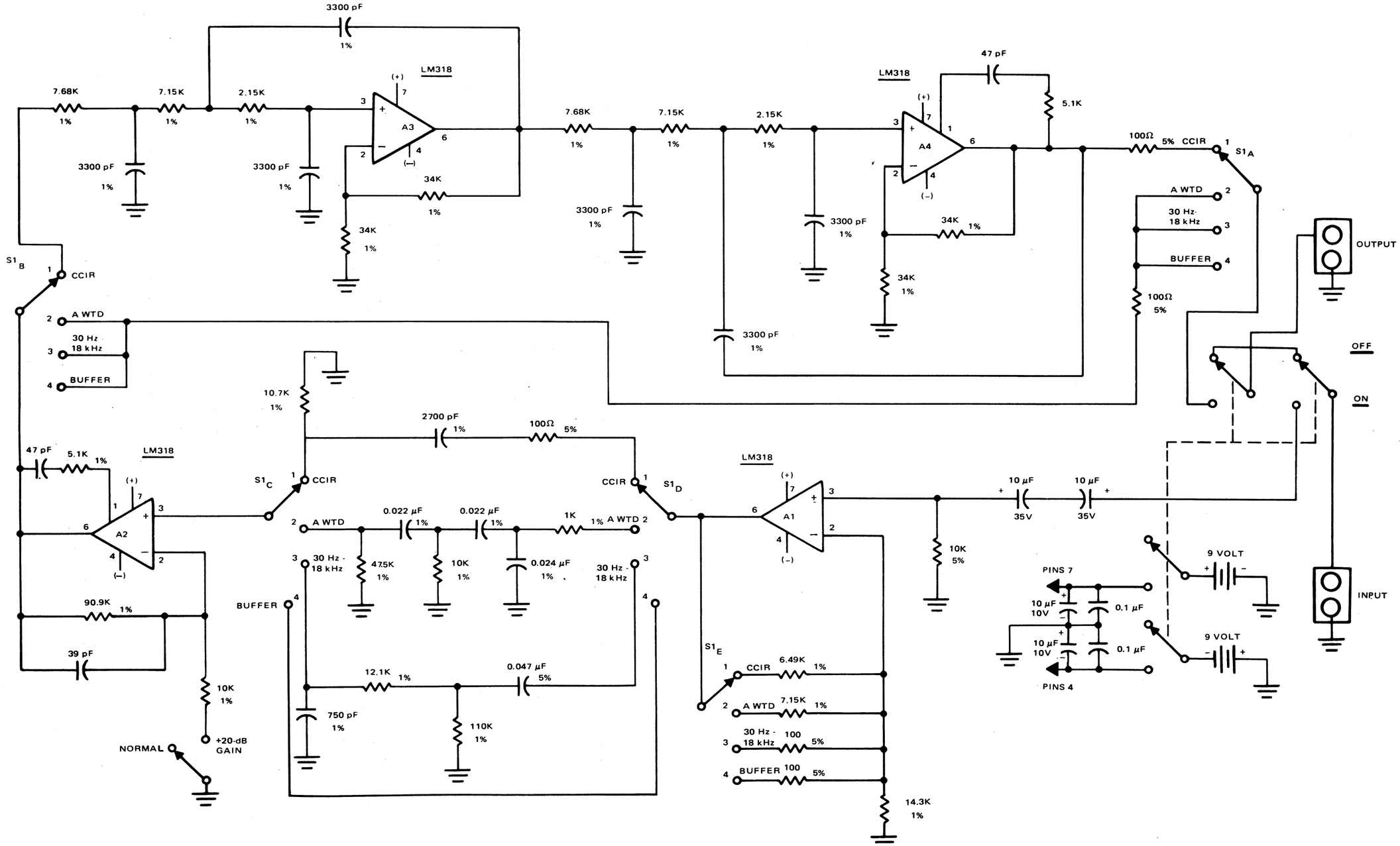


Figure 5-35.
Universal Noise Filter Schematic

Table 5-14. Overall Signal-to-Noise Ratio Specifications

TAPE SPEED AND EQUALIZATION	TRACK FORMAT	30 Hz – 18 kHz UNWEIGHTED	ANSI "A" WEIGHTED	CCIR REC 468 WEIGHTED
30 in/s AES	Full Track	77 dB	81 dB	73 dB
	2-Track and 4-Track	72 dB	76 dB	67 dB
15 in/s IEC/CCIR	Full Track	74 dB	78 dB	70 dB
	2-Track and 4-Track	70 dB	74 dB	65 dB
15 in/s NAB	Full -Track	73 dB	77 dB	69 dB
	2-Track and 4-Track	69 dB	73 dB	63 dB
7.5 in/s NAB	Full Track	75 dB	78 dB	70 dB
	2-Track and 4-Track	71 dB	74 dB	63 dB
7.5 in/s IEC/CCIR	Full Track	71 dB	76 dB	67 dB
	2-Track and 4-Track	68 dB	71 dB	62 dB
3.75 in/s IEC/NAB*	Full Track	68 dB	72 dB	64 dB
	2-Track and 4-Track	64 dB	66 dB	57 dB

*At 3.75 in/s, overall signal-to-noise ratio is measured with respect to a record level of 740 nWb/m (6 dB above operating level of 370 nWb/m). At 740 nWb/m, mid-frequency, third harmonic distortion is less than 3%.

All signal-to-noise ratio figures given are with respect to a level 9 dB above 370 nWb/m when using Ampex 456 tape or its direct equivalent.

Table 5-15. Typical Standby Signal-to-Noise Ratio Specifications

TAPE SPEED AND EQUALIZATION	TRACK FORMAT	30 Hz – 18 kHz UNWEIGHTED	ANSI "A" WEIGHTED	CCIR REC 468 WEIGHTED
30 in/s AES	Full Track	82 dB	90 dB	88 dB
	2-Track and 4-Track	78 dB	86 dB	85 dB
15 in/s IEC/CCIR or NAB	Full Track	80 dB	90 dB	84 dB
	2-Track and 4-Track	76 dB	86 dB	80 dB
7.5 in/s IEC/CCIR or NAB	Full Track	78 dB	86 dB	82 dB
	2-Track and 4-Track	75 dB	83 dB	76 dB
3.75 in/s IEC/NAB*	Full Track	74 dB	80 dB	77 dB
	2-Track and 4-Track	70 dB	76 dB	70 dB

*At 3.75 in/s, overall signal-to-noise ratio is measured with respect to a record level of 740 nWb/m (6 dB above operating level of 370 nWb/m). At 740 nWb/m, mid-frequency, third harmonic distortion is less than 3%.

All signal-to-noise ratio figures given are with respect to a level 9 dB above 370 nWb/m when using Ampex 456 tape or its direct equivalent.

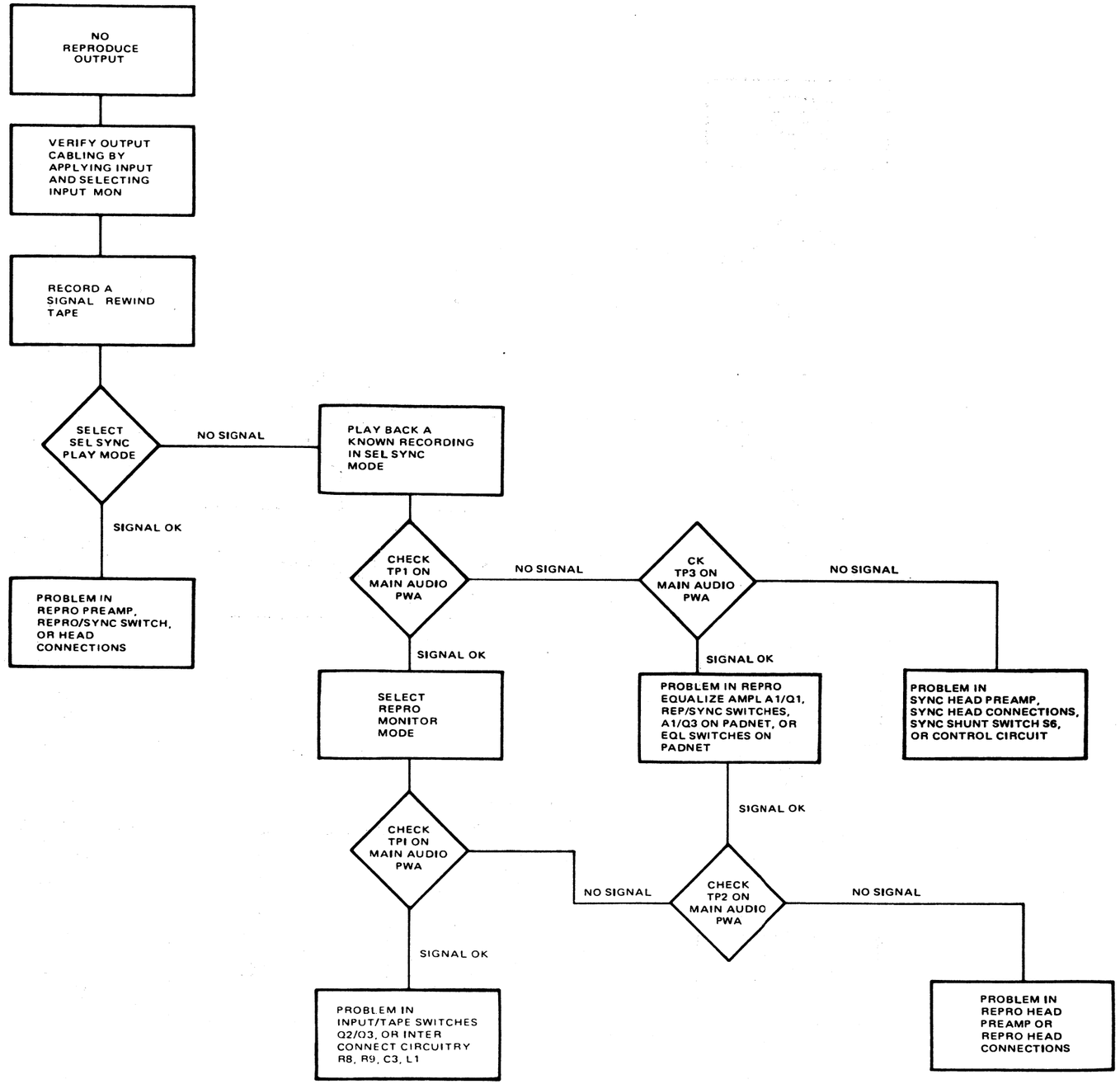


Figure 5-41.
No Reproduce Output-
Troubleshooting Flow Chart

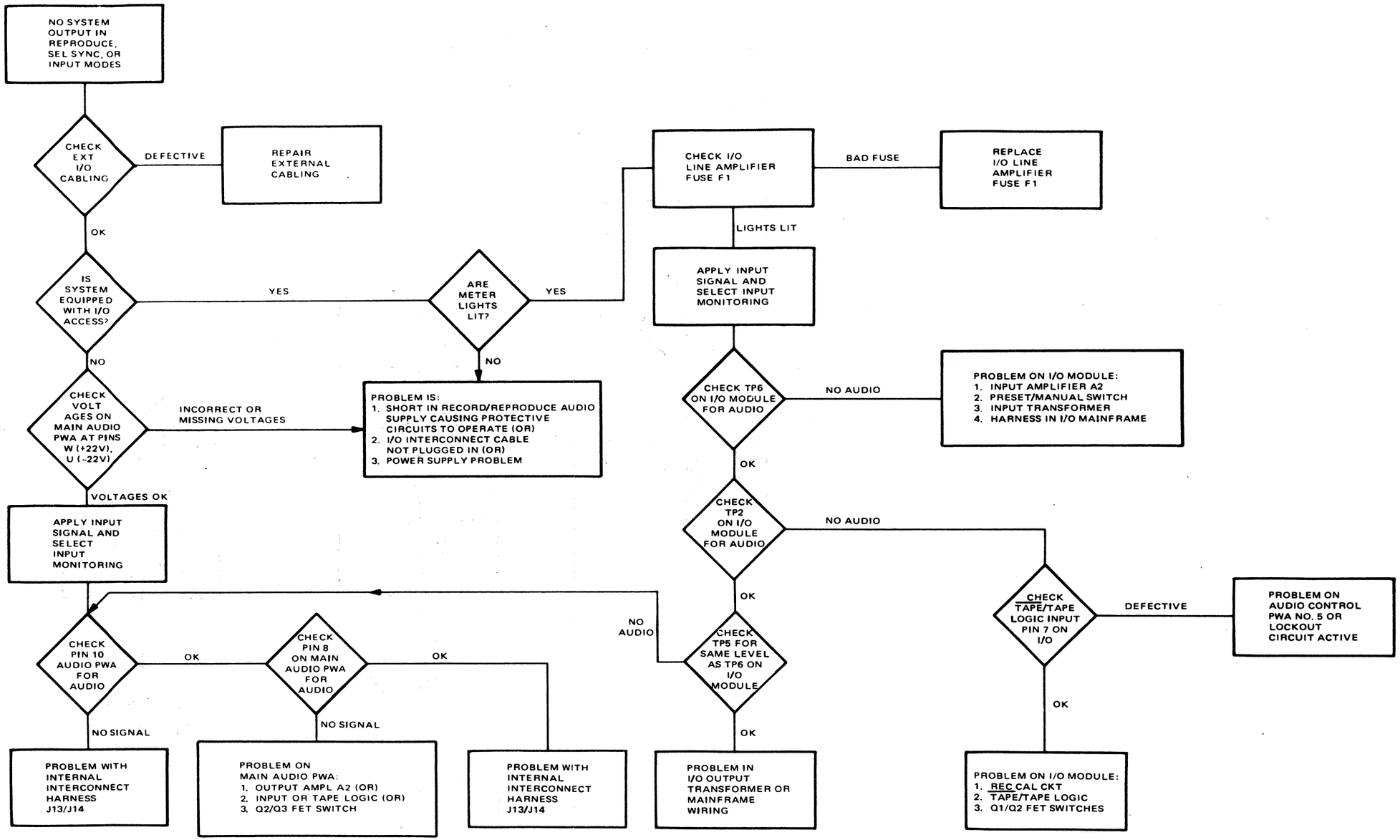


Figure 5-42.
No System Output in Reproduce, Sel-Sync, or Input Modes Troubleshooting Flow Chart

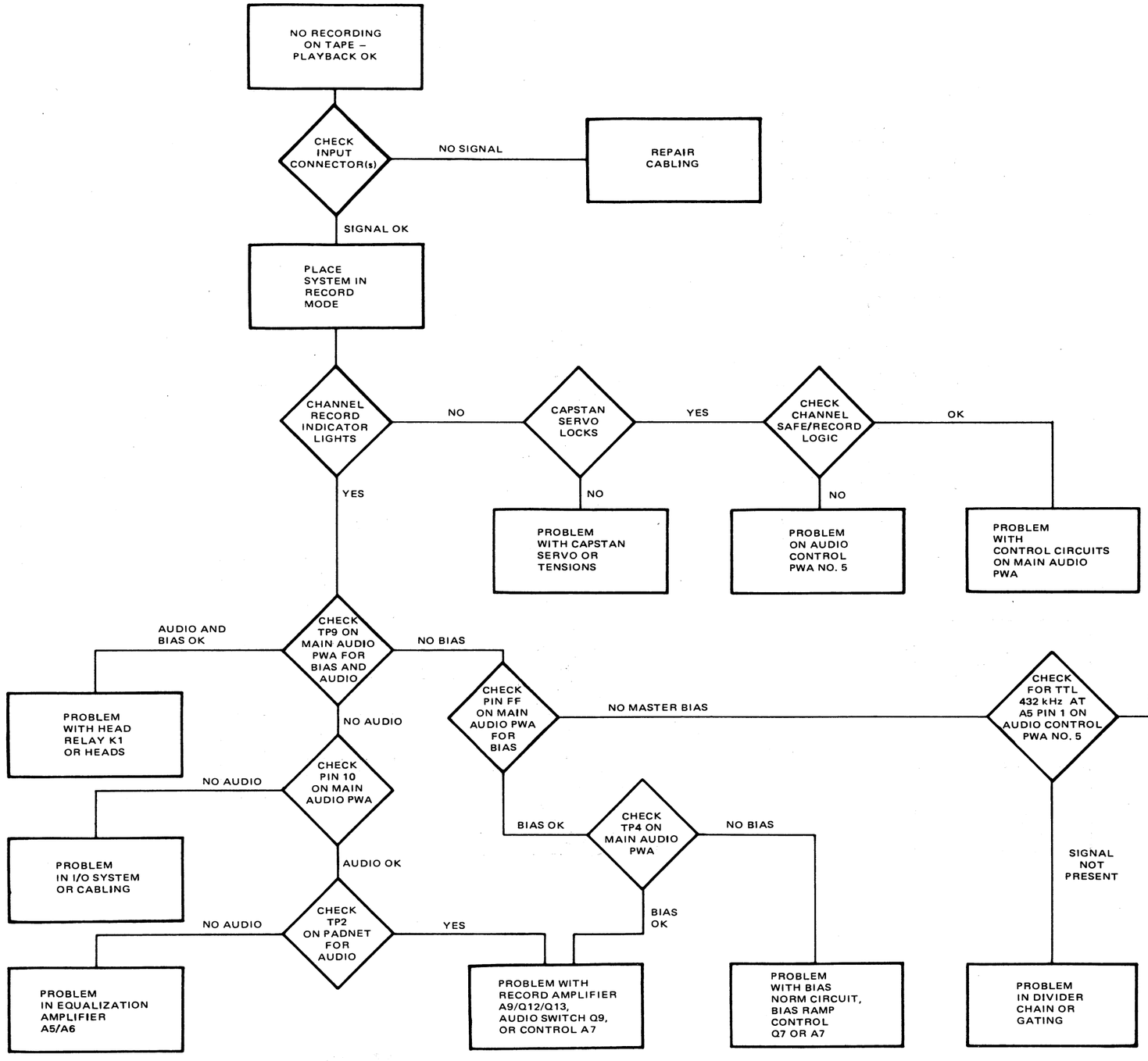


Figure 5-43.
No Recording on Tape-
Troubleshooting Flow Chart

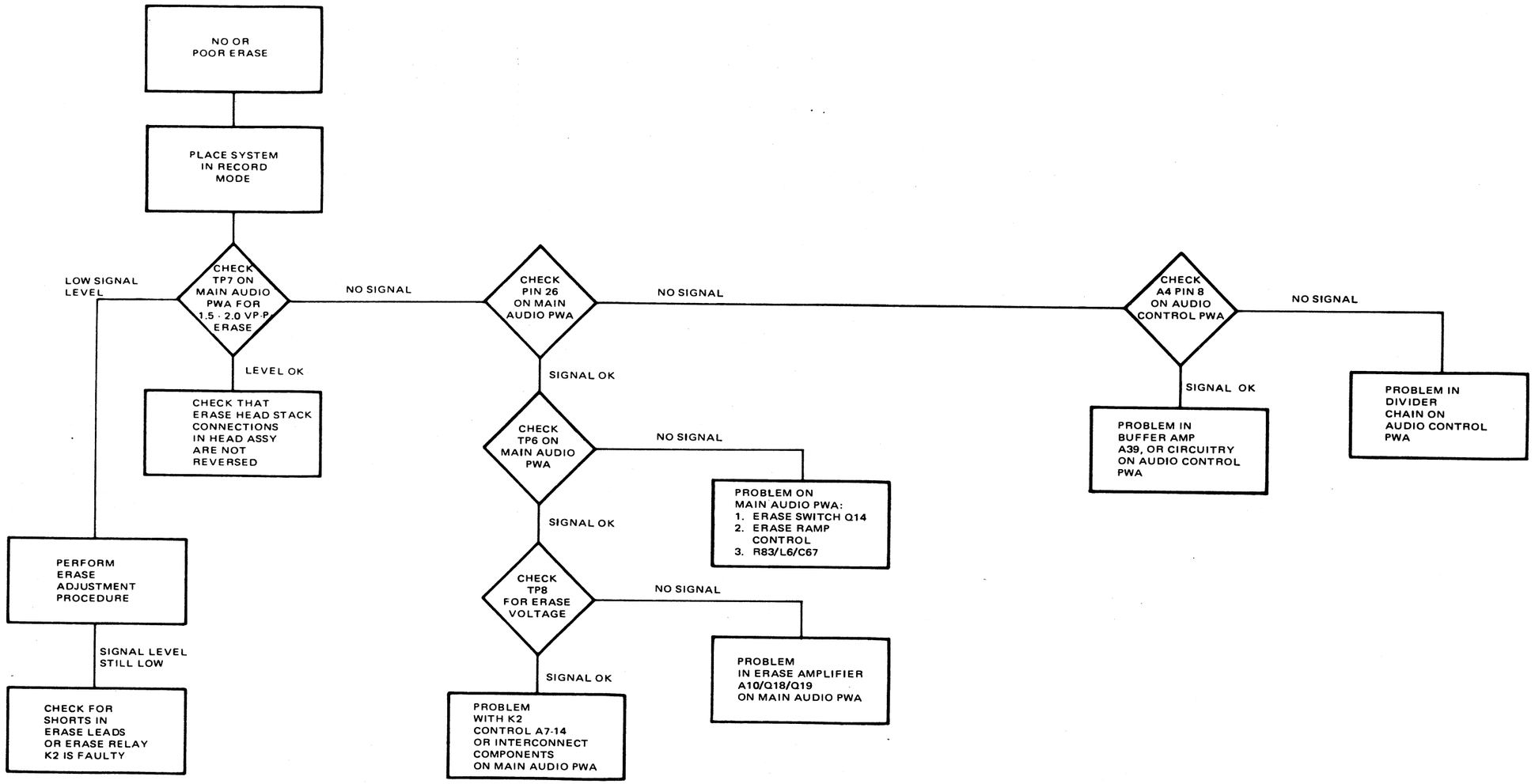
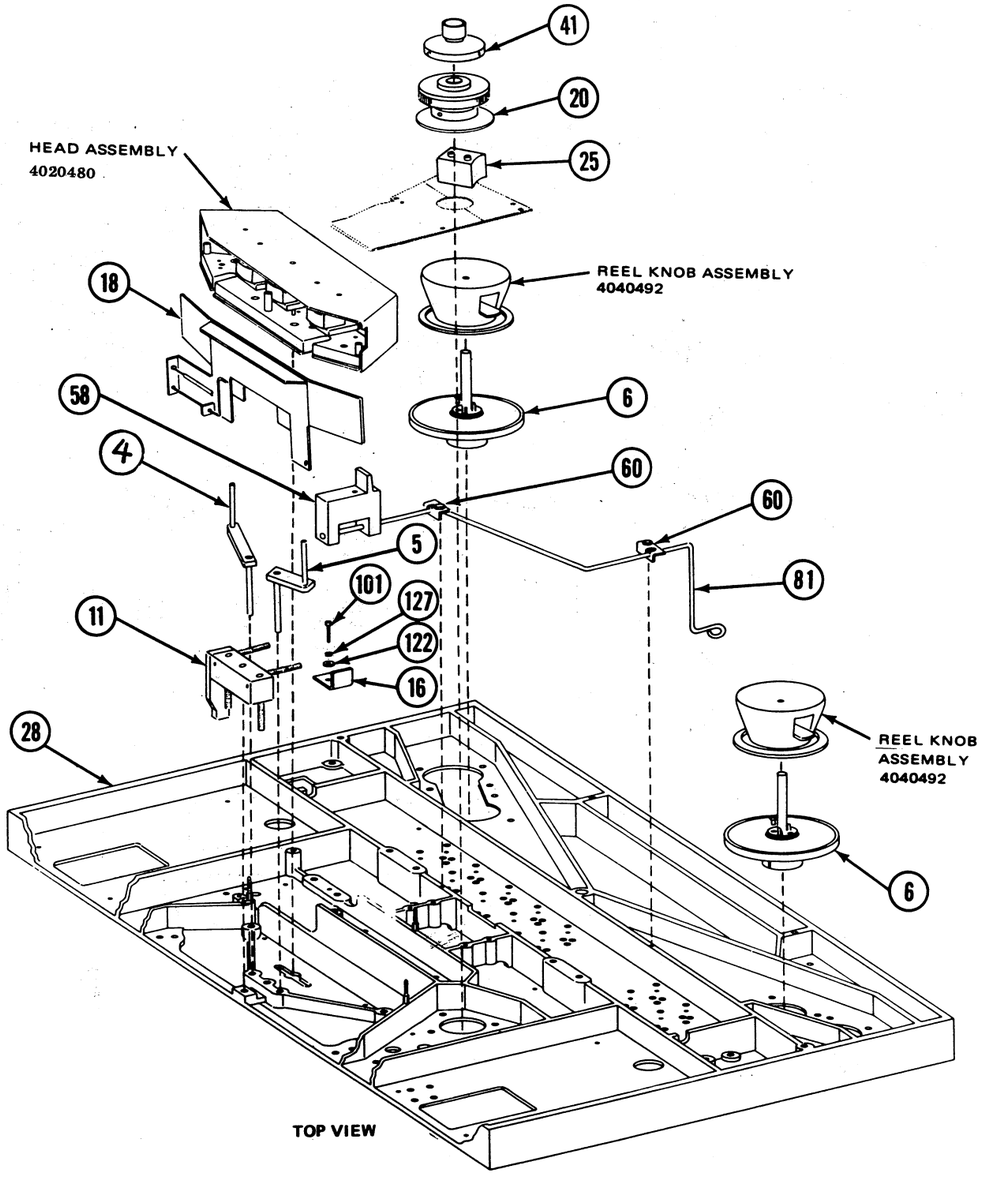
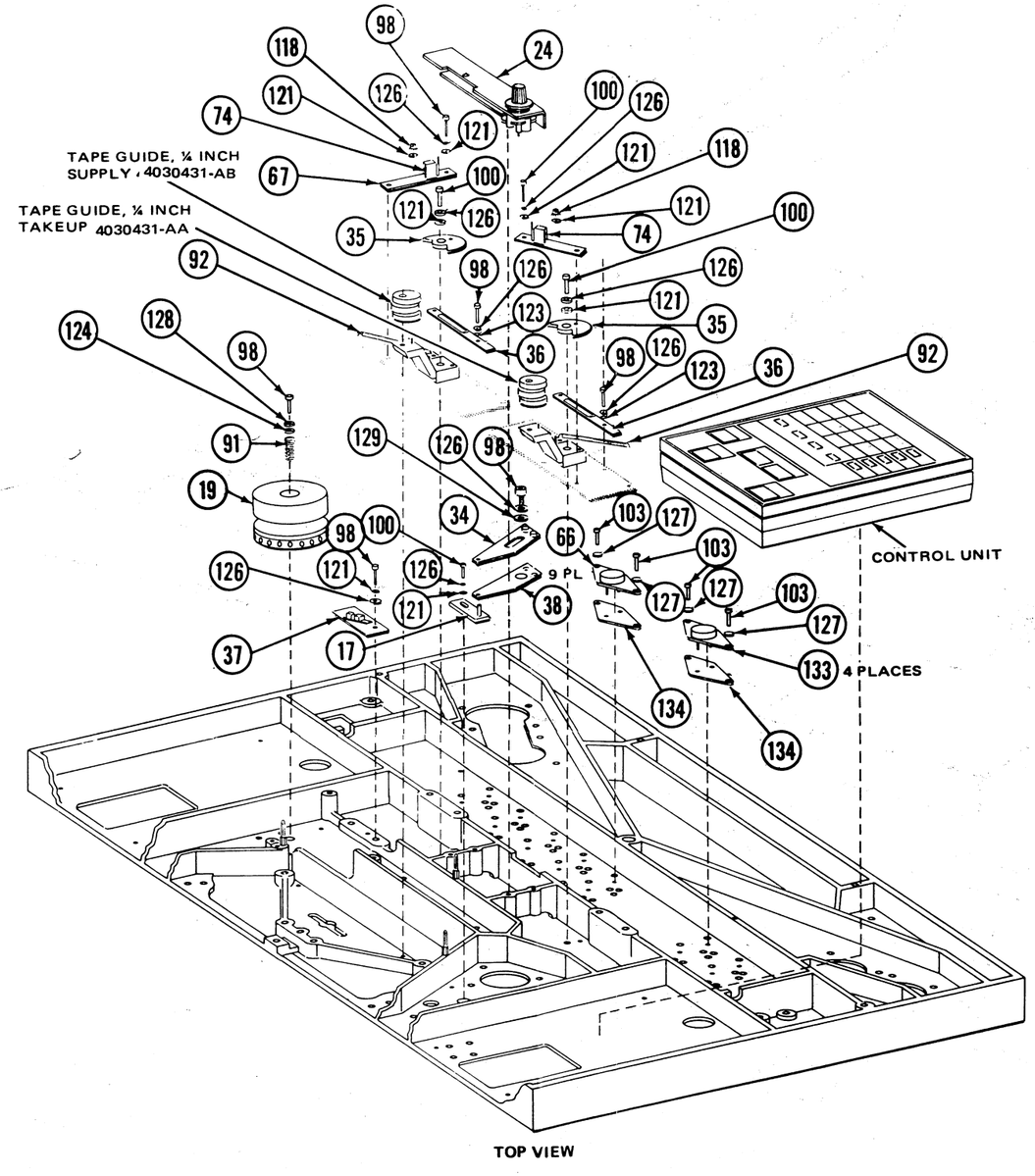
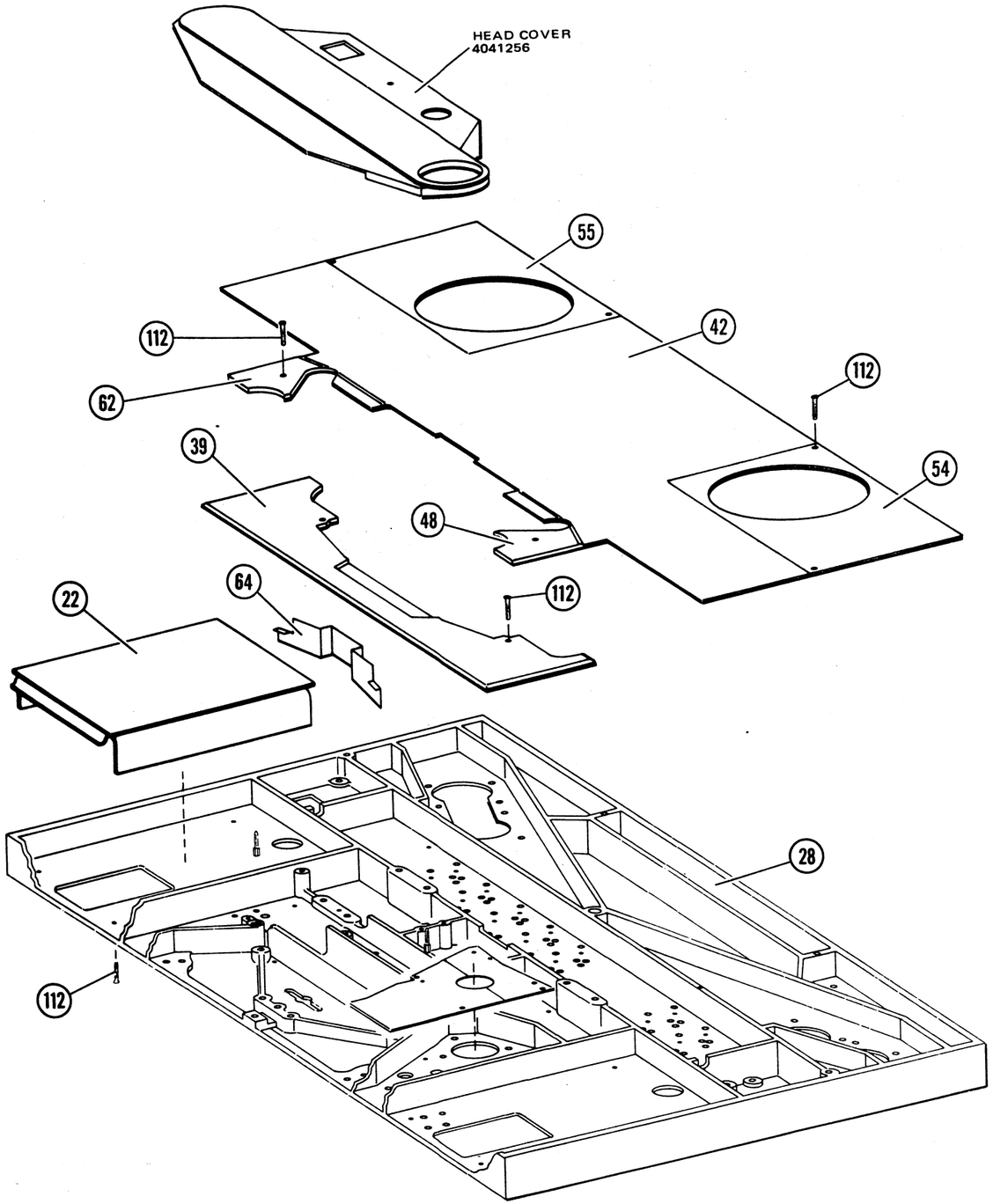


Figure 5-44.
No or Poor Erase-
Troubleshooting Flow Chart

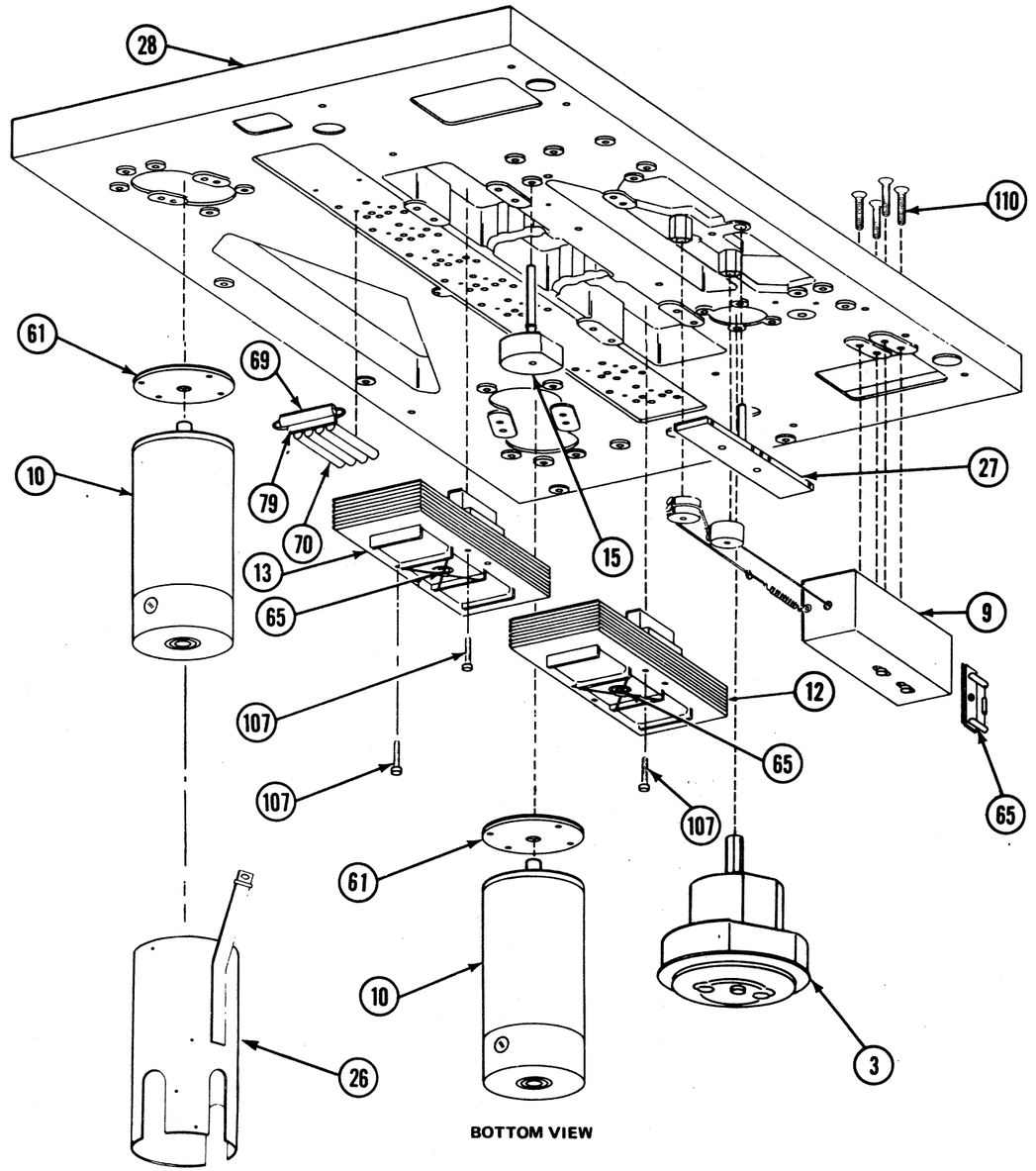




Assembly No. 4020434.
Transport Assembly
(Sheet 1 of 2)

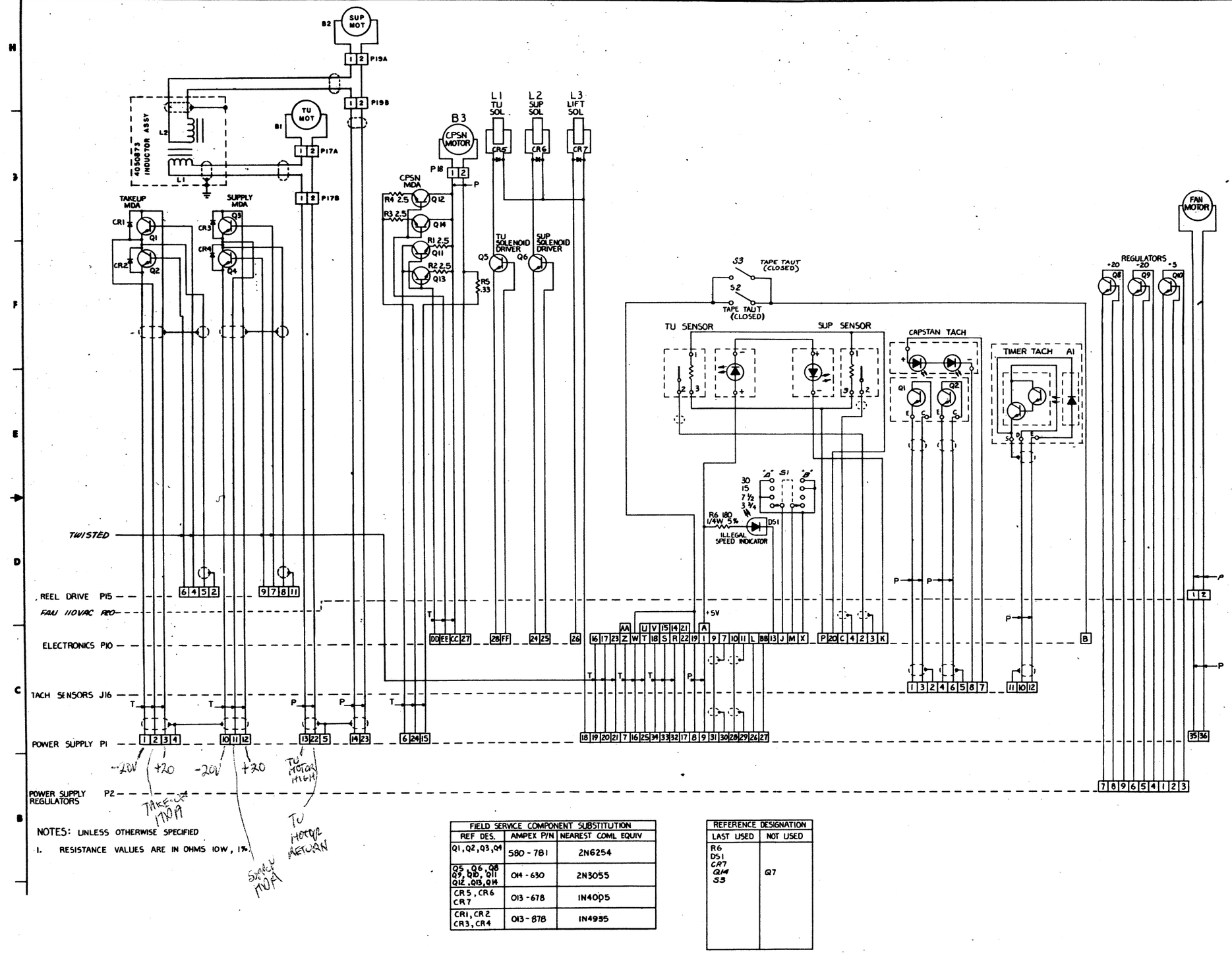


TOP VIEW



BOTTOM VIEW

Assembly No. 4020434.
Transport Assembly
(Sheet 2 of 2)



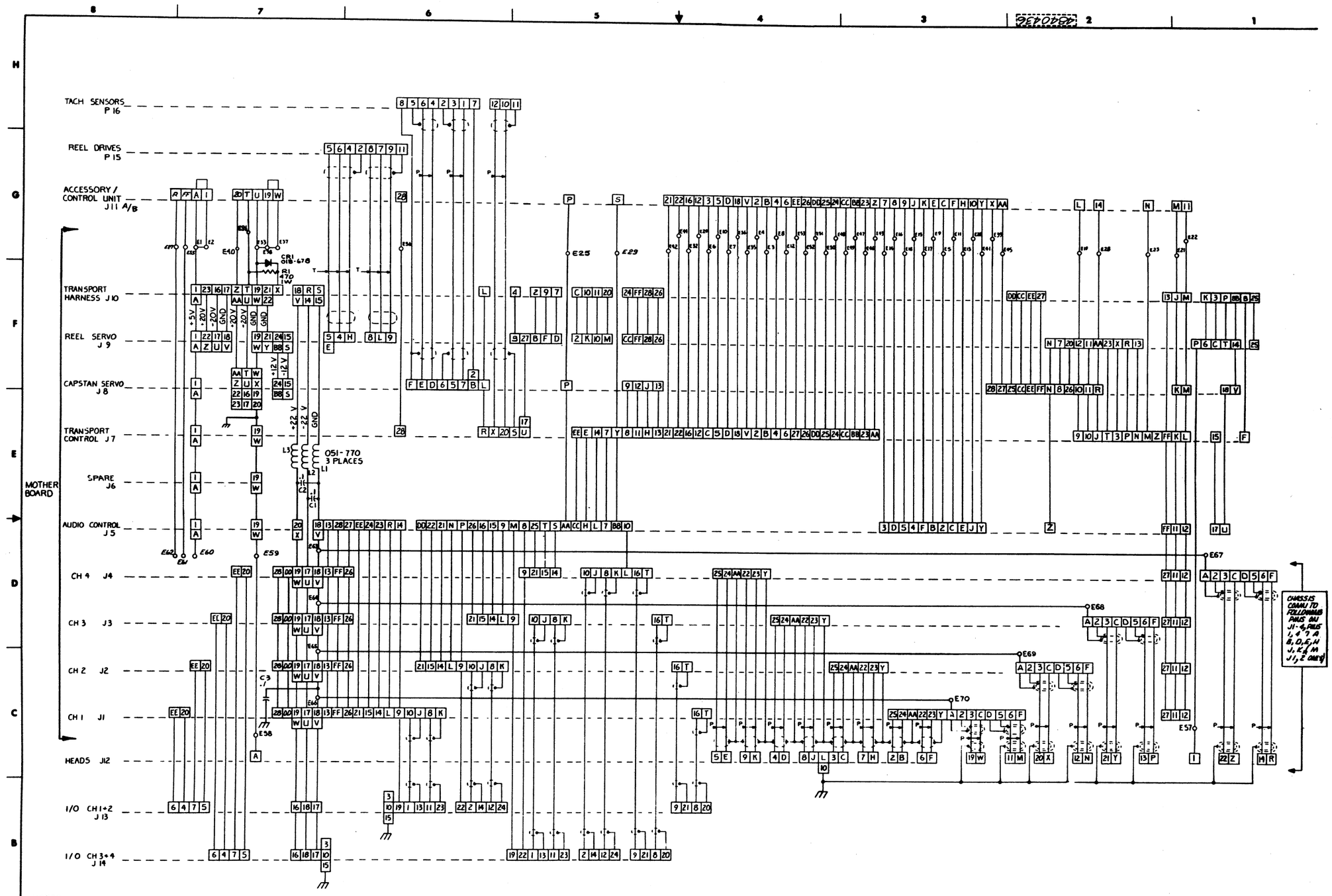
NOTES: UNLESS OTHERWISE SPECIFIED

1. RESISTANCE VALUES ARE IN OHMS 10W, 1%

FIELD SERVICE COMPONENT SUBSTITUTION		
REF DES.	AMPEX P/N	NEAREST COML EQUIV
Q1, Q2, Q3, Q4	580 - 781	2N6254
Q5, Q6, Q8 Q9, Q10, Q11 Q12, Q13, Q14	014 - 630	2N3055
CR5, CR6 CR7	013 - 678	IN4005
CR1, CR2 CR3, CR4	013 - 878	IN4935

REFERENCE DESIGNATION	
LAST USED	NOT USED
R6	
D51	
CR7	
Q14	Q7
S3	

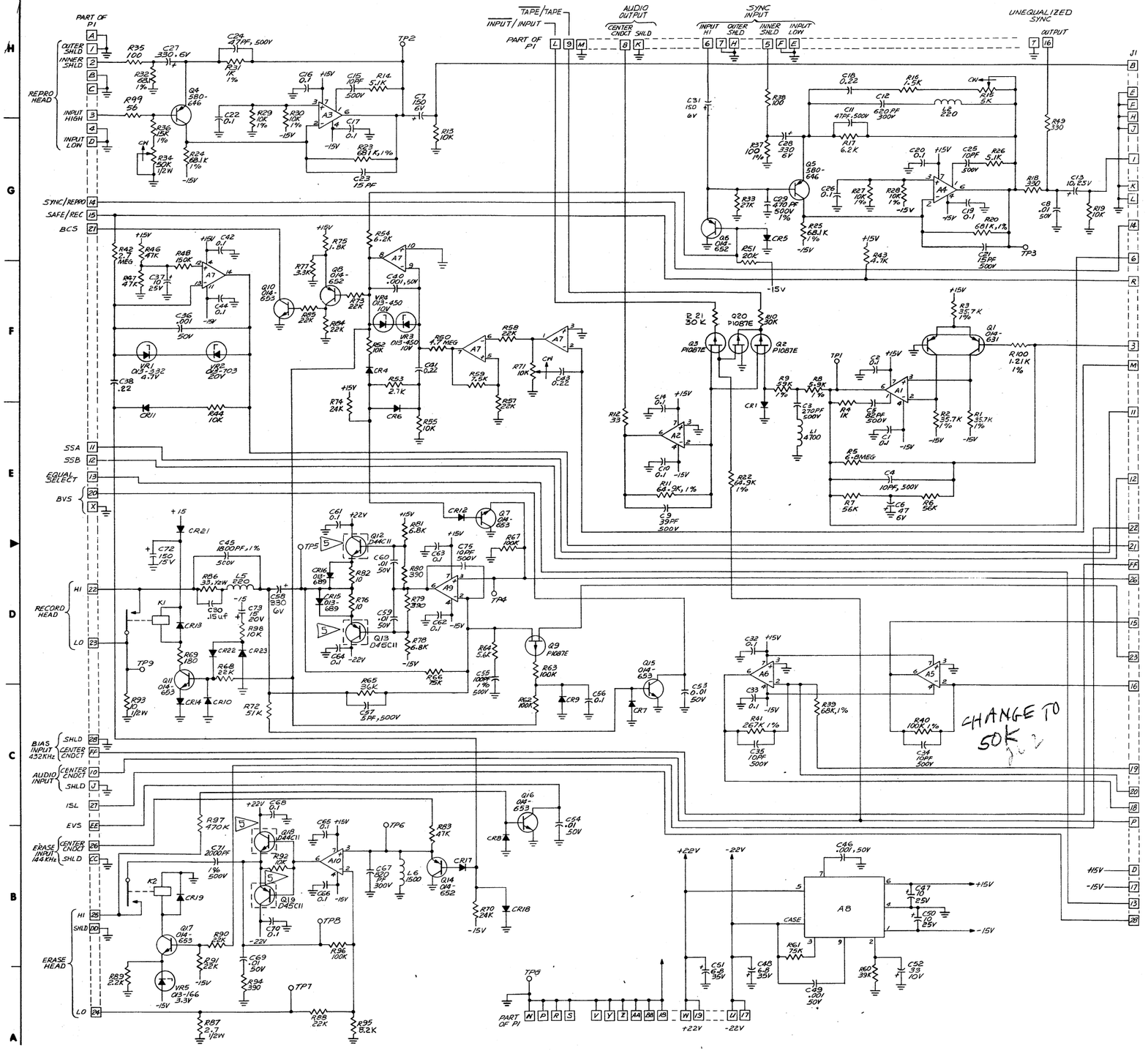
Schematic No. 4840423E.
Transport Assembly Interconnect Diagram



NOTES: UNLESS OTHERWISE SPECIFIED.

1. RESISTANCE VALUES ARE IN OHMS, 5%
2. CAPACITANCE VALUES ARE IN MICROFARADS, 50V.

Wiring Diagram No. 4840436C.
Electronic Wiring Diagram



FIELD SERVICE COMPONENT SUBSTITUTION LIST	
AMPEX P/N	NEAREST COMMERCIAL EQUIVALENT
014-652	2N3906
014-653	2N3904
580-646	2N3764

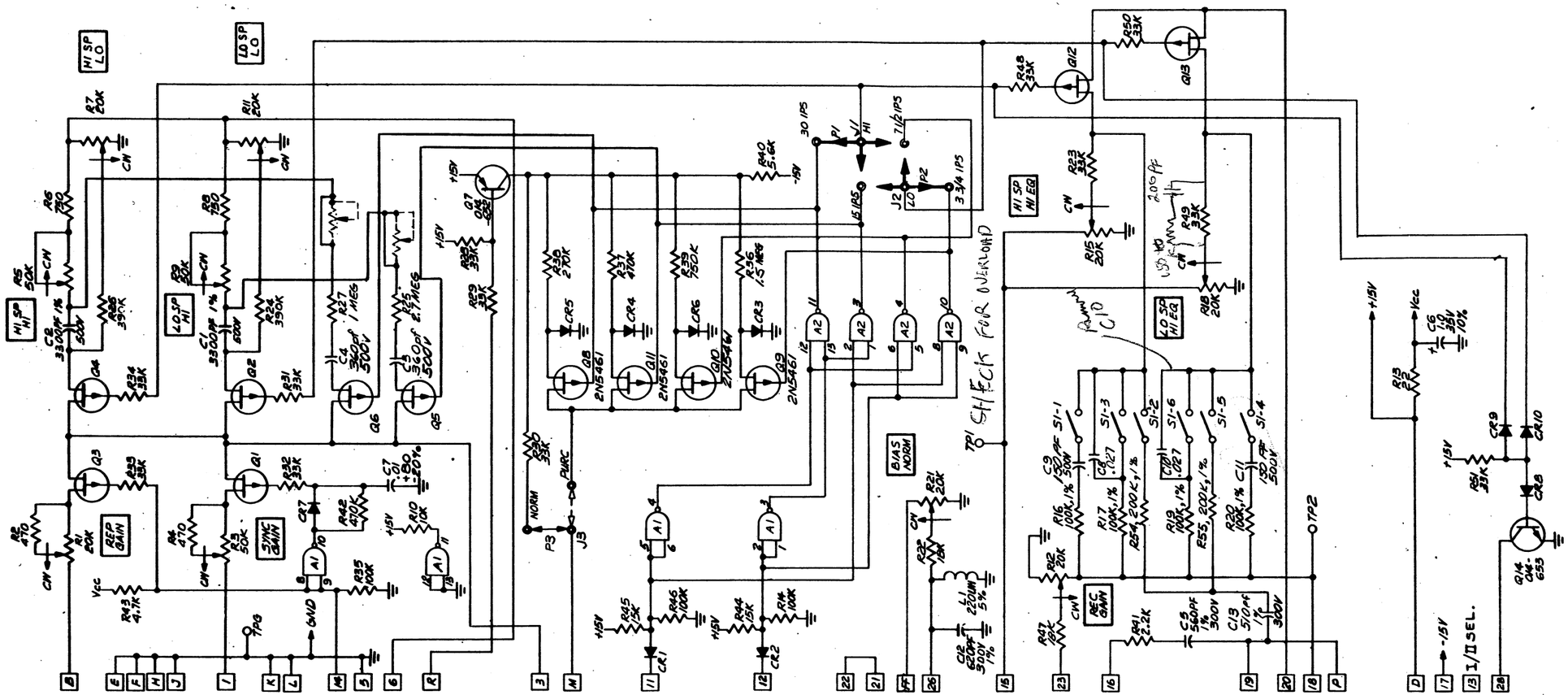
IC LIST			
REF DES	A7	A1-6, 9, 10	A8
AMPEX P/N	589-428	587-478	587-701
VENDOR P/N	TLO84CN	LM318H	RC4194TK

NOTES: UNLESS OTHERWISE SPECIFIED

1. CAPACITANCE VALUES ARE IN MICROFARADS, 100V.
2. DIODES ARE TYPE 013-539
3. INDUCTANCE VALUES ARE IN MICROHENRIES.
4. RESISTANCE VALUES ARE IN OHMS, 1/4 W, 5%.
5. THESE TRANSISTORS HAVE HEATSINKS
6. PWA NO. IS 40507S4-16

REFERENCE DESIGNATIONS	
LAST USED	NOT USED
A10	
C75	C39,74
CR23	CR22,5,20
J1	
K2	
L6	L3,4
P1	
Q20	
R100	
TP9, TP6	R45,R56
VR5	

Schematic No. 4840378S.
Main Audio PWA, Nos. 1, 2, 3 and 4



SPEED SELECT JUMPER CHART	
HI SPEED	LO SPEED
J1 - 30 IPS	J2 - 15 IPS
J1 - 15 IPS	J2 - 7½ IPS
J1 - 7½ IPS	J2 - 3¾ IPS

PRESET RECORD EQUALIZATION		
S1-1	SHELF DOWN	HI SPEED
S1-2	SHELF UP	
S1-3	3180/∞	
S1-4	SHELF DOWN	LO SPEED
S1-5	SHELF UP	
S1-6	3180/∞	

NOTES: UNLESS OTHERWISE SPECIFIED

1. CAPACITANCE VALUES ARE IN MICROFARADS, 50V, 5%
2. DIODES ARE AMPEX P/N 013-599
3. RESISTANCE VALUES ARE IN OHMS, ¼W, 5%.
4. TRANSISTORS ARE TYPE P10B7E
5. INTEGRATED CIRCUITS ARE TYPE 4011, PIN 14 TO Vcc, PIN 7 TO GROUND.
6.

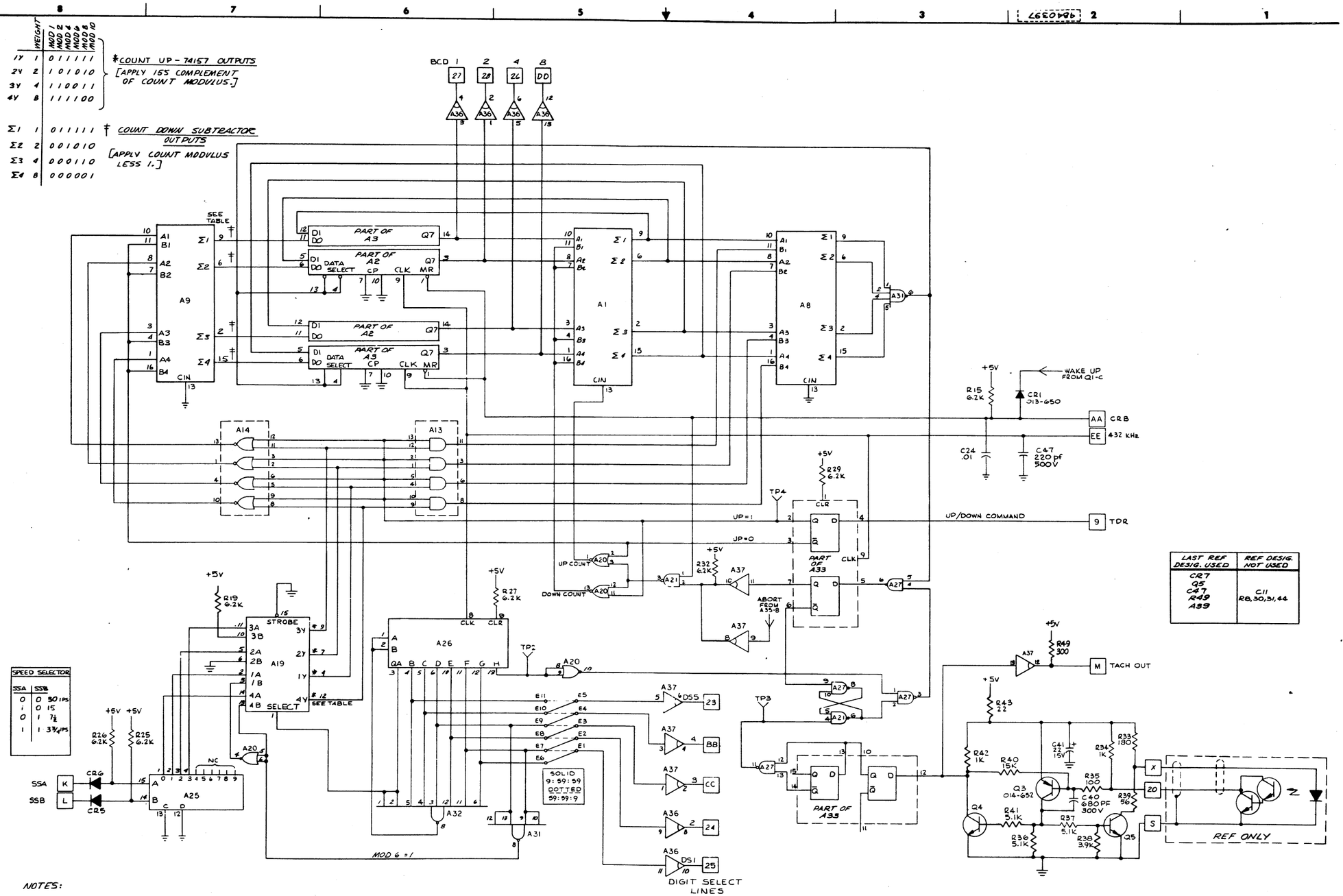
FIELD SERVICE COMPONENT SUBSTITUTION LIST	
AMPEX P/N	NEAREST COMMERCIAL EQUIVALENT
014-652	2N3906
014-653	2N3904

7. J1 & J2 SHOWN CONNECTED FOR 30 IPS HIGH SPEED AND 3 3/4 IPS LOW SPEED.

REFERENCE DESIGNATIONS	
LAST USED	NOT USED
A2 C13 J3 Q14 R65 S1 TP2, TPG CR10	R58, 59

Schematic No. 4840379D.
PADNET PWA

6-79/6-80



NOTES:

UNLESS OTHERWISE SPECIFIED:

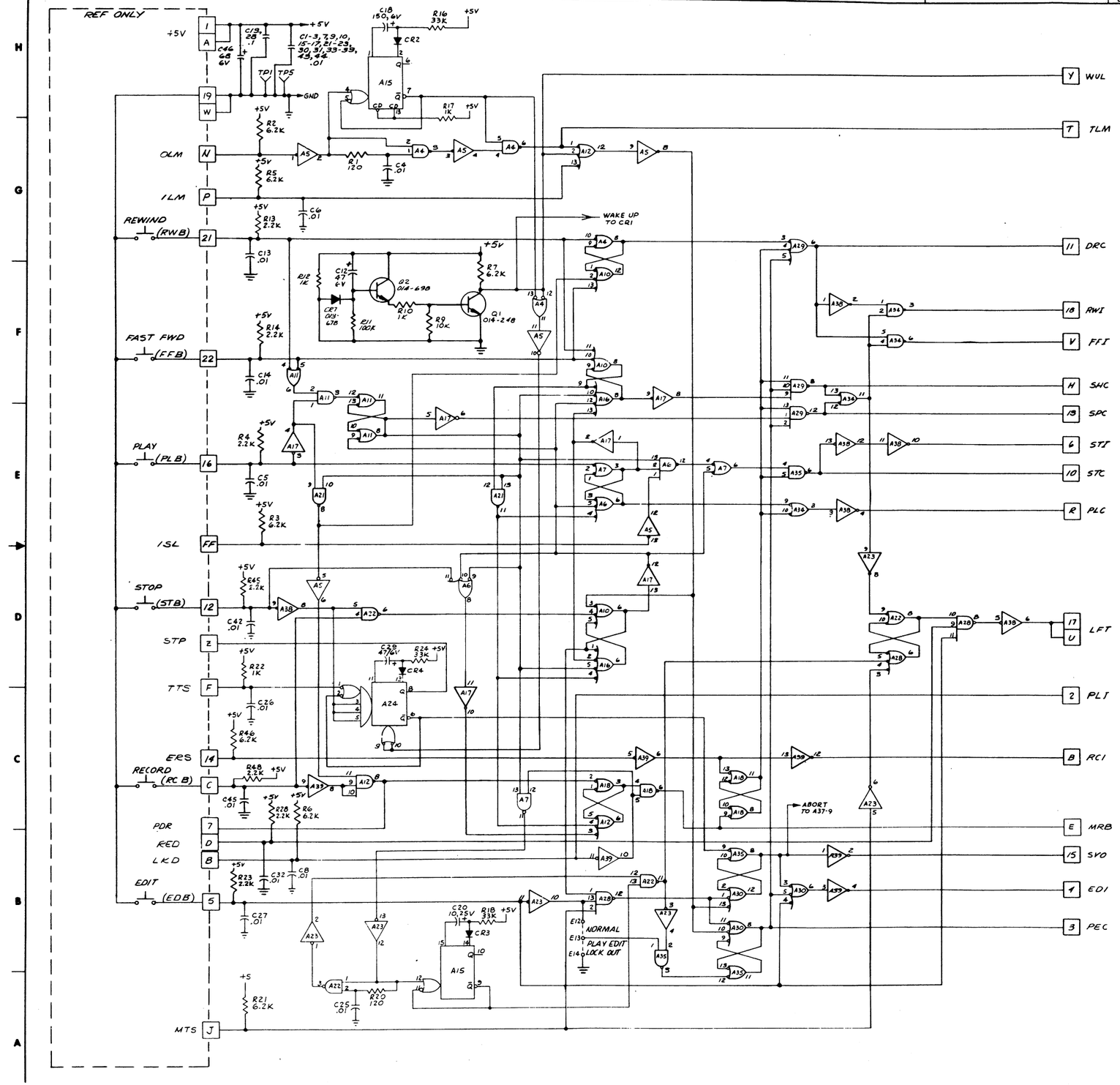
1. ALL RESISTOR VALUES ARE IN OHMS, 1/4W, 5%.
2. ALL CAPACITOR VALUES ARE IN MICROFARADS, 50V.
3. ALL DIODES ARE 013-599.
4. ALL TRANSISTORS ARE 014-653.
5. SCHEMATIC REFLECTS PWA 4050787-06.

REFERENCE DESIGNATION	A4, 7, 11, 18, 21, 22, 27, 34, 35	A14, 20	A5, 17, 23, 38 39	A13	A6, 10, 12, 28, 29, 30	A36, 37	A16, 31	A32
AMPEX PART NO.	586-075	586-109	586-326	586-759	586-076	586-890	586-077	586-078
VENDOR PART NO.	7400	7402	7404	7408	7410	7417	7420	7430
VCC +5V PIN	14	14	14	14	14	14	14	14
GND PIN	7	7	7	7	7	7	7	7

REFERENCE DESIGNATION	A25	A26	A1, 8, 9	A19	A33	A2, 3	A24	A15
AMPEX PART NO.	586-423	586-450	586-554	586-903	586-925	586-303	587-416	587-144
VENDOR PART NO.	7442	74164	7483	74157	74175	9328	9600	9602
VCC +5V PIN	16	14	5	16	16	16	14	16
GND PIN	8	7	12	8	8	8	7	8

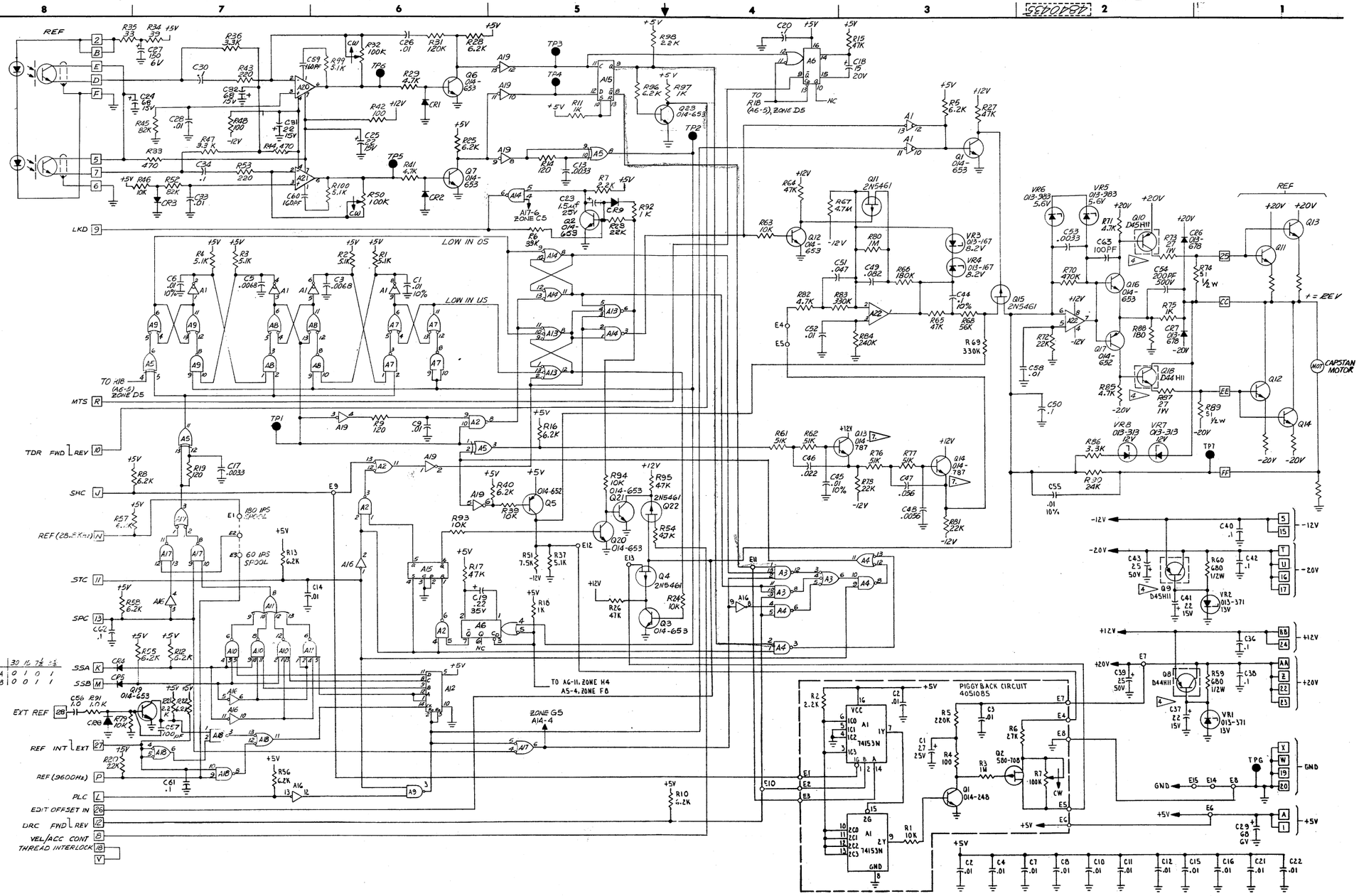
Schematic No. 4840397F.
Transport Logic and Tape Timer PWA, No. 7
(Sheet 1 of 2)

6-91/6-92



Schematic No. 4840397E.
Transport Logic and Tape Timer PWA, No. 7
(Sheet 2 of 2)

6-93/6-94

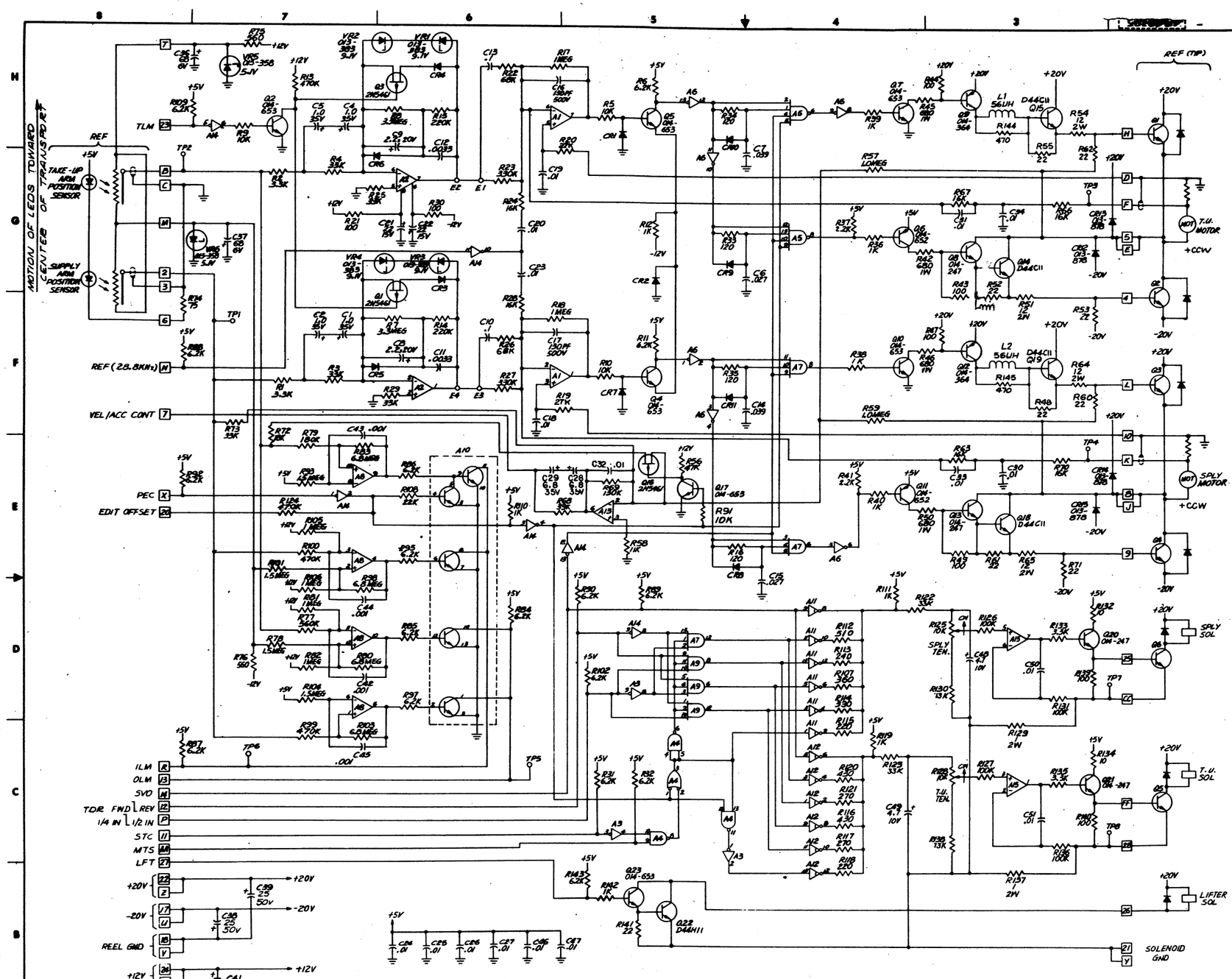


INTEGRATED CIRCUIT LIST				
REFERENCE DESIGNATION	AMPEX P/N	VENDOR P/N	VOLTAGE PIN +5V	GROUND PIN
A2,4,7,8,9,14,17,18	586-075	7400	14	7
A3,10,13	586-076	7410	14	7
A11	586-077	7420	14	7
A15	586-108	7474	14	7
A20,21	587-178	318H	4 (-12V) 7 (+12V)	NONE
A12	586-283	7493	5	10
A1	586-325	7405	14	7
A16,19	586-326	7404	14	7
A5	586-705	7486	14	7
A22	586-905	1458	4 (-12V) 8 (+12V)	NONE
A6	587-144	9602	16	8

REFERENCE DESIGNATIONS	
LAST USED	NOT USED
A22	
CG3	C35
E15	
Q23	R38
R100	
CR9	
VR8	
TR7	
TP8	

NOTES: UNLESS OTHERWISE SPECIFIED
1. CAPACITANCE VALUES ARE IN MICROFARADS, 50V.
2. DIODES ARE TYPE 013-599.
3. RESISTANCE VALUES ARE IN OHMS, 1/4W, 5%.
4. THESE TRANSISTORS TO HAVE HEATSINK.
5. ALL LOGIC INPUT LEVELS ARE LOW TRUE.
6. PWA IS 4050840-08.
7. PART NO. 014-862 MAY BE SUBSTITUTED.

Schematic No. 4840435N.
Capstan Servo PWA, No. 8

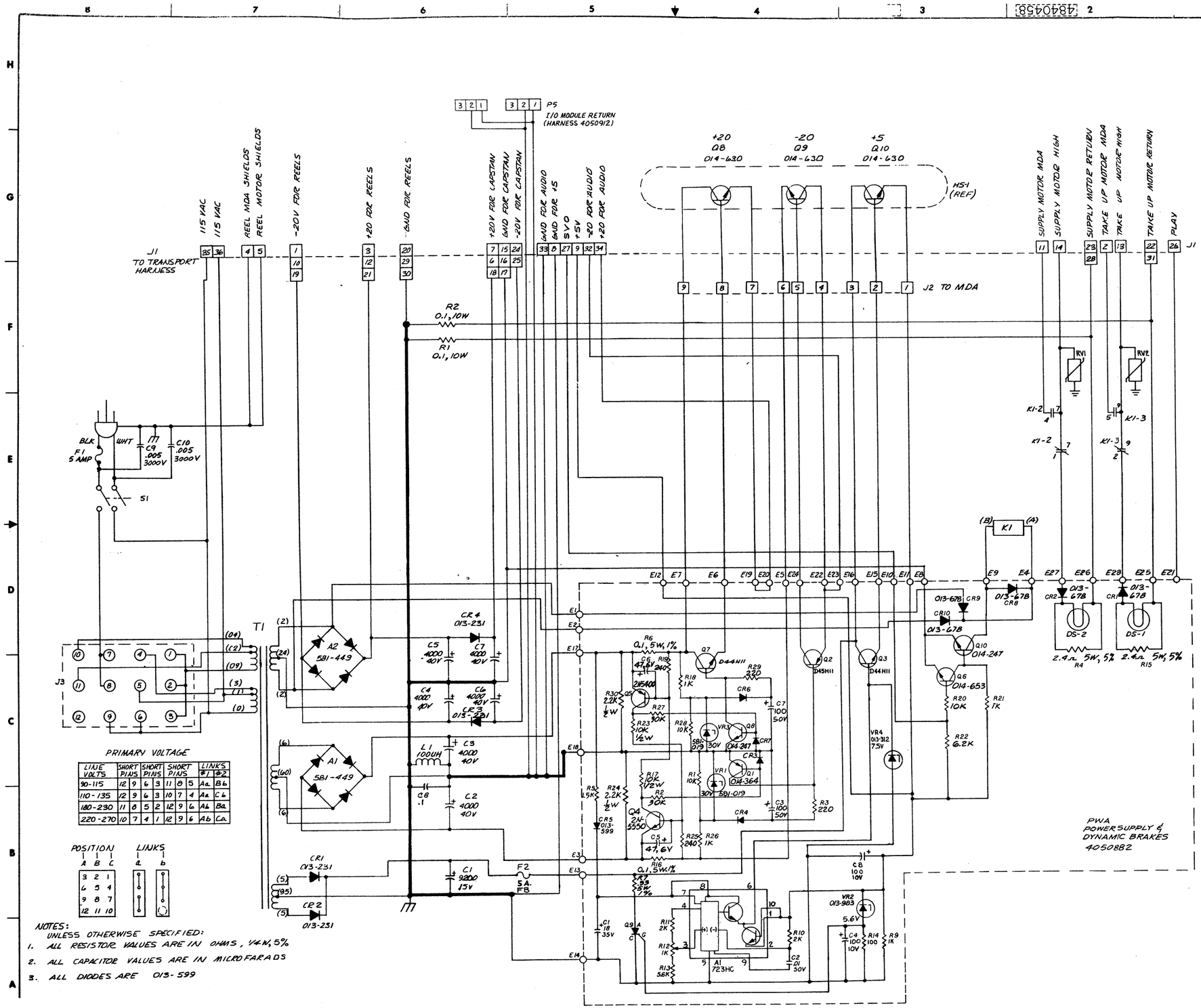


FIELD SERVICE COMPONENT SUBSTITUTION		
REF DES	AMPEX P/N	COMMERCIAL EQUIVALENT
Q5, 13, 20, 21	014-247	2N2219
Q9, 12	014-364	2N2905A
Q6, 11	014-652	2N3906
Q2, 4, 5, 7, 10, 17, 23	014-653	2N3904

INTEGRATED CIRCUIT LIST					
REFERENCE DESIGNATION	AMPEX P/N	VENDOR P/N	VOLTAGE PIN	GROUND PIN	
A4	586-075	7400	14	7	
A5	586-077	7420	14	7	
A13	586-269	M741	7 (+V) 4 (-V)	NONE	
A10	586-276	3046	NONE	NONE	
A11, 12	586-325	7405	14	7	
A3, 6, 14	586-326	7404	14	7	
A1, 2, 15	586-905	M558	8 (+V) 4 (-V)	NONE	
A7, 9	687-598	7411A	14	7	
A8	687-714	3900	14	7	

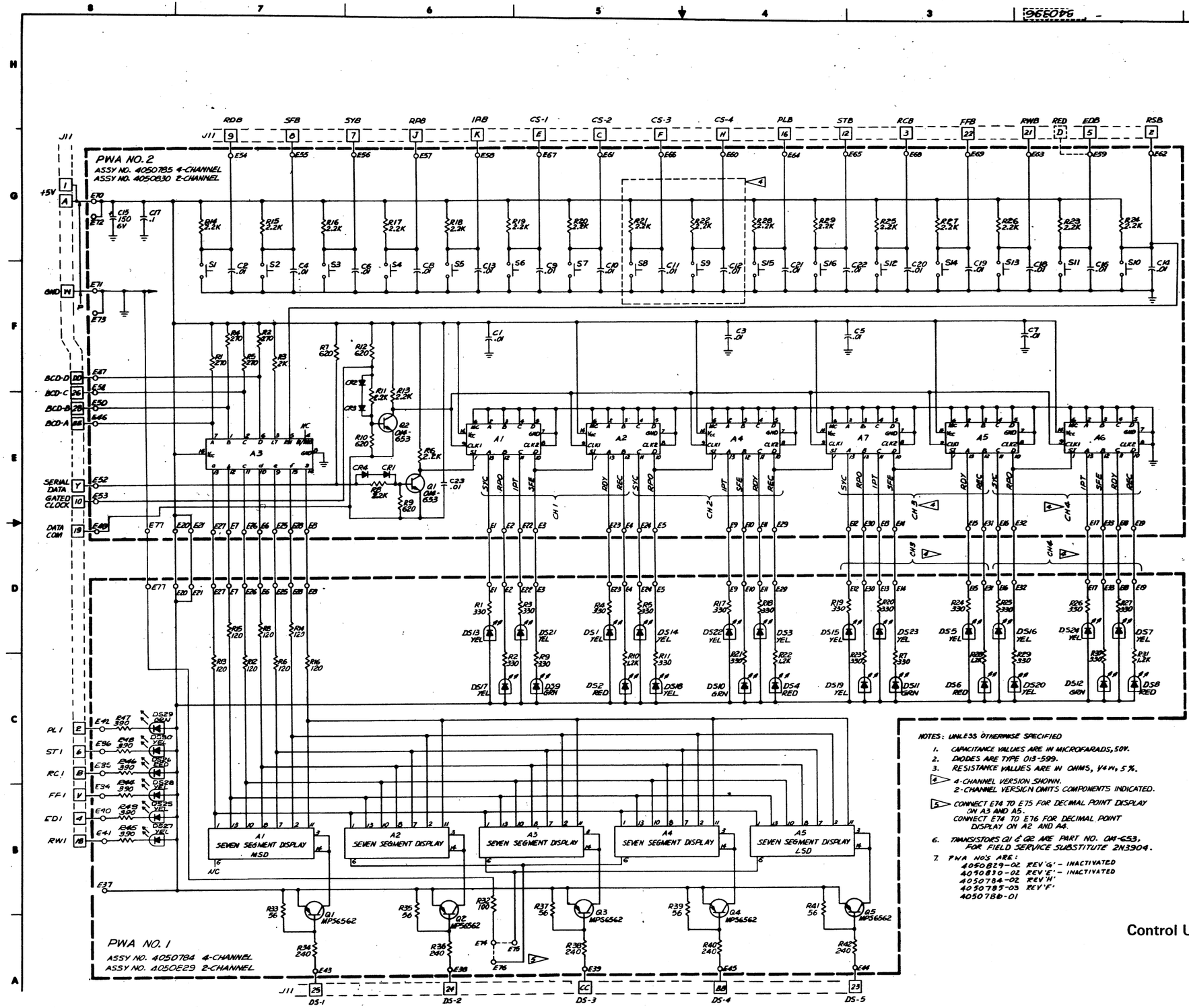
REFERENCE DESIGNATIONS	
LAST USED	NOT USED
A15	C3
C51	R94, 96
E4	
Q23	
R145	
TP8	
TP9	
CR15	
VR6	
L2	

Schematic No. 4840395L.
Reel Servo PWA, No. 9



NOTES:
UNLESS OTHERWISE SPECIFIED:
1. ALL RESISTOR VALUES ARE IN OHMS, 1/4W, 5%
2. ALL CAPACITOR VALUES ARE IN MICROFARADS
3. ALL DIODES ARE 013-599

Schematic No. 4840458G.
Power Supply and Dynamic Brakes PWA



REF. DESIG.	
LAST USED	NOT USED
R29	
A7	
CR4	
CR3	
816	
E77	E34-165 & E74-76

IC LIST		
REF DES	A1 A2 A4 A5 A6 A7	A3
AMPEX P/N	586-785	587-544
VENDOR P/N	7495	7447

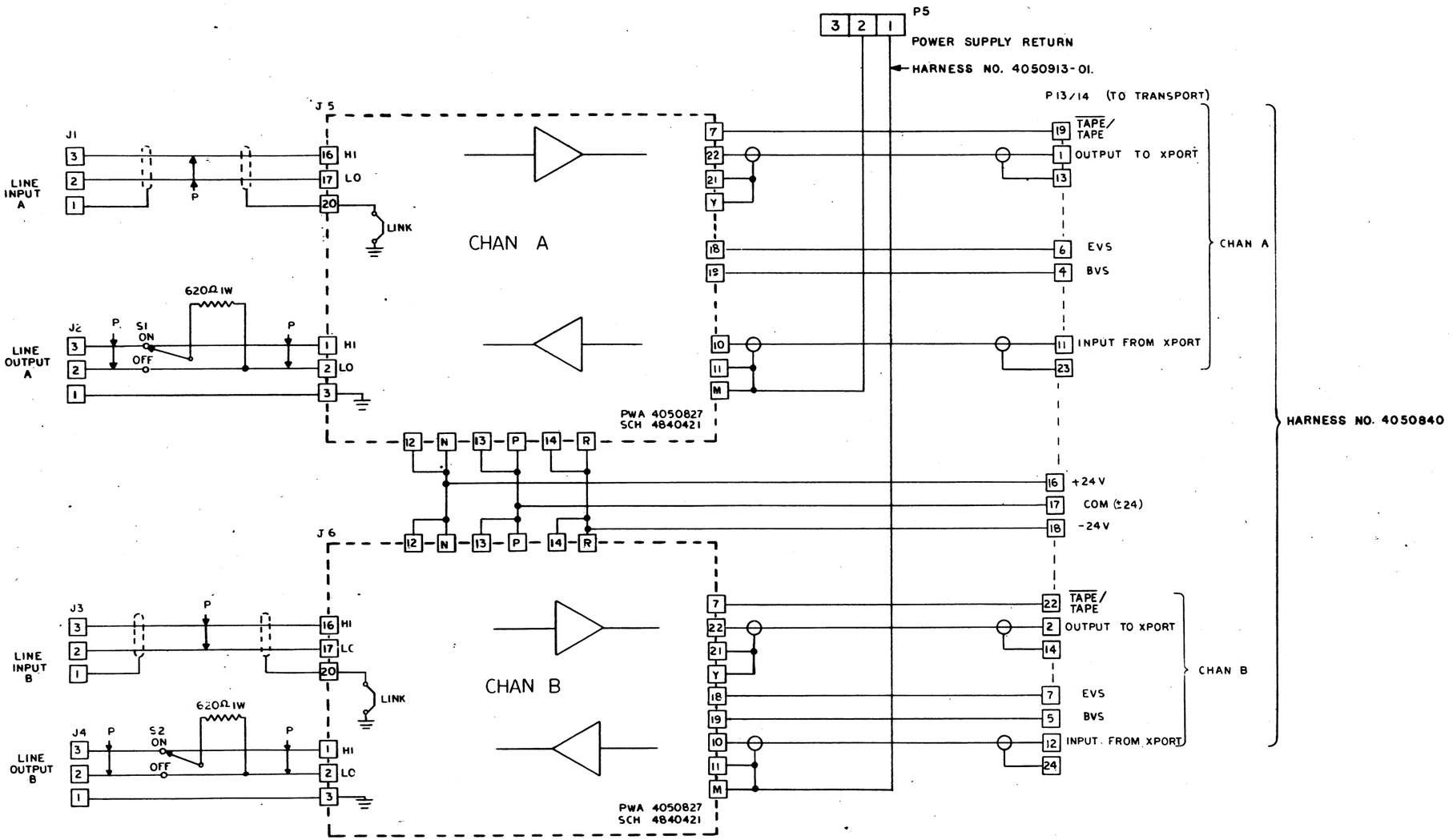
REF.	DESIG.
LAST USED	NOT USED
D380	
Q15	
A6	
R48	
E77	E46-E78

IC LIST	
REF DES	A1-5
AMPEX P/N	581-957
VENDOR P/N	5082-7730

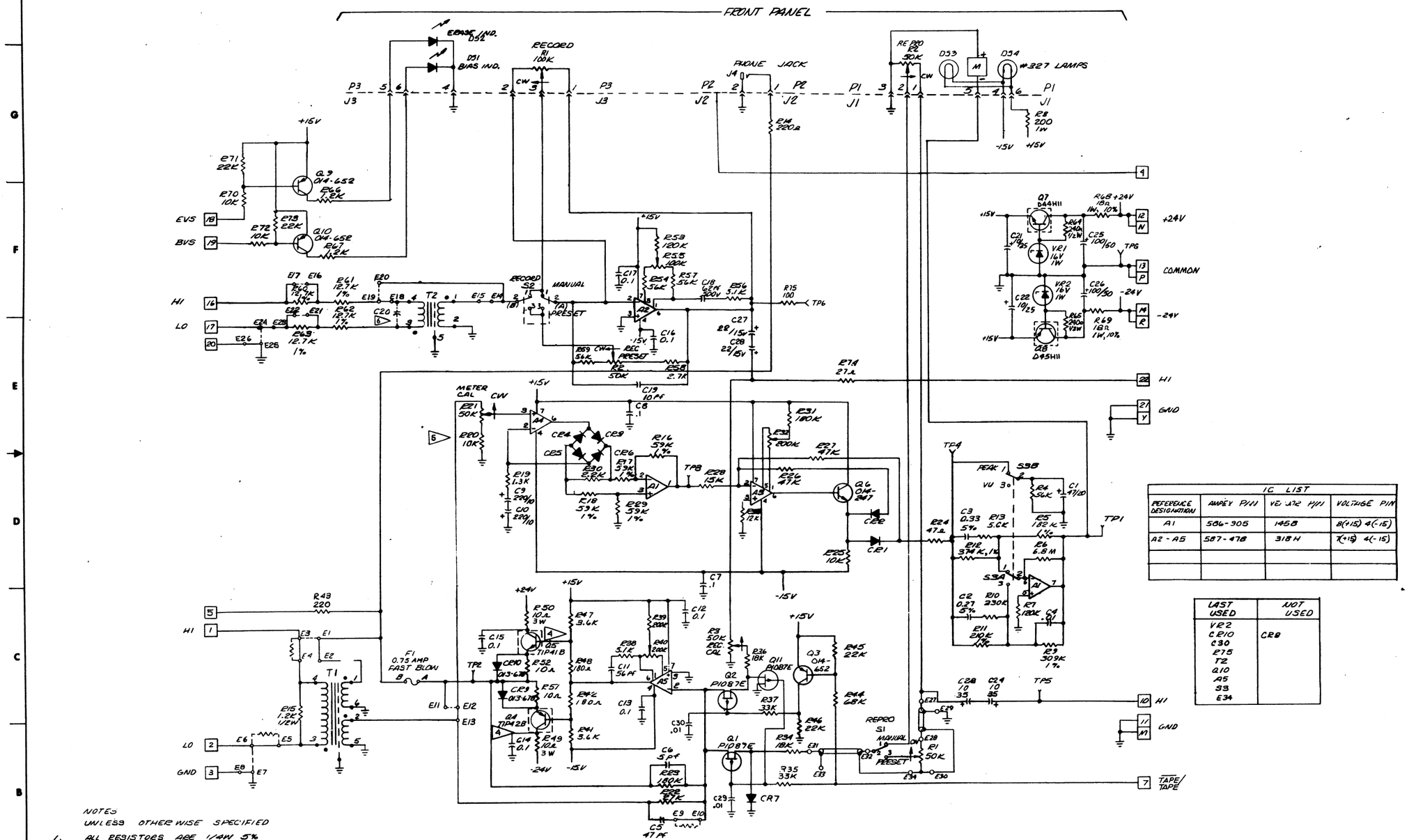
NOTES: UNLESS OTHERWISE SPECIFIED

1. CAPACITANCE VALUES ARE IN MICROFARADS, 50V.
2. DIODES ARE TYPE 013-599.
3. RESISTANCE VALUES ARE IN OHMS, ¼W, 5%.
4. 4-CHANNEL VERSION SHOWN. 2-CHANNEL VERSION OMITS COMPONENTS INDICATED.
5. CONNECT E74 TO E75 FOR DECIMAL POINT DISPLAY ON A3 AND A5. CONNECT E74 TO E76 FOR DECIMAL POINT DISPLAY ON A2 AND A4.
6. TRANSISTORS Q1 & Q2 ARE PART NO. CM-653, FOR FIELD SERVICE SUBSTITUTE 2N3904.
7. PWA NO'S ARE:
   4050829-02 REV 'G' - INACTIVATED
   4050830-02 REV 'E' - INACTIVATED
   4050784-02 REV 'H'
   4050785-03 REV 'F'
   4050788-01

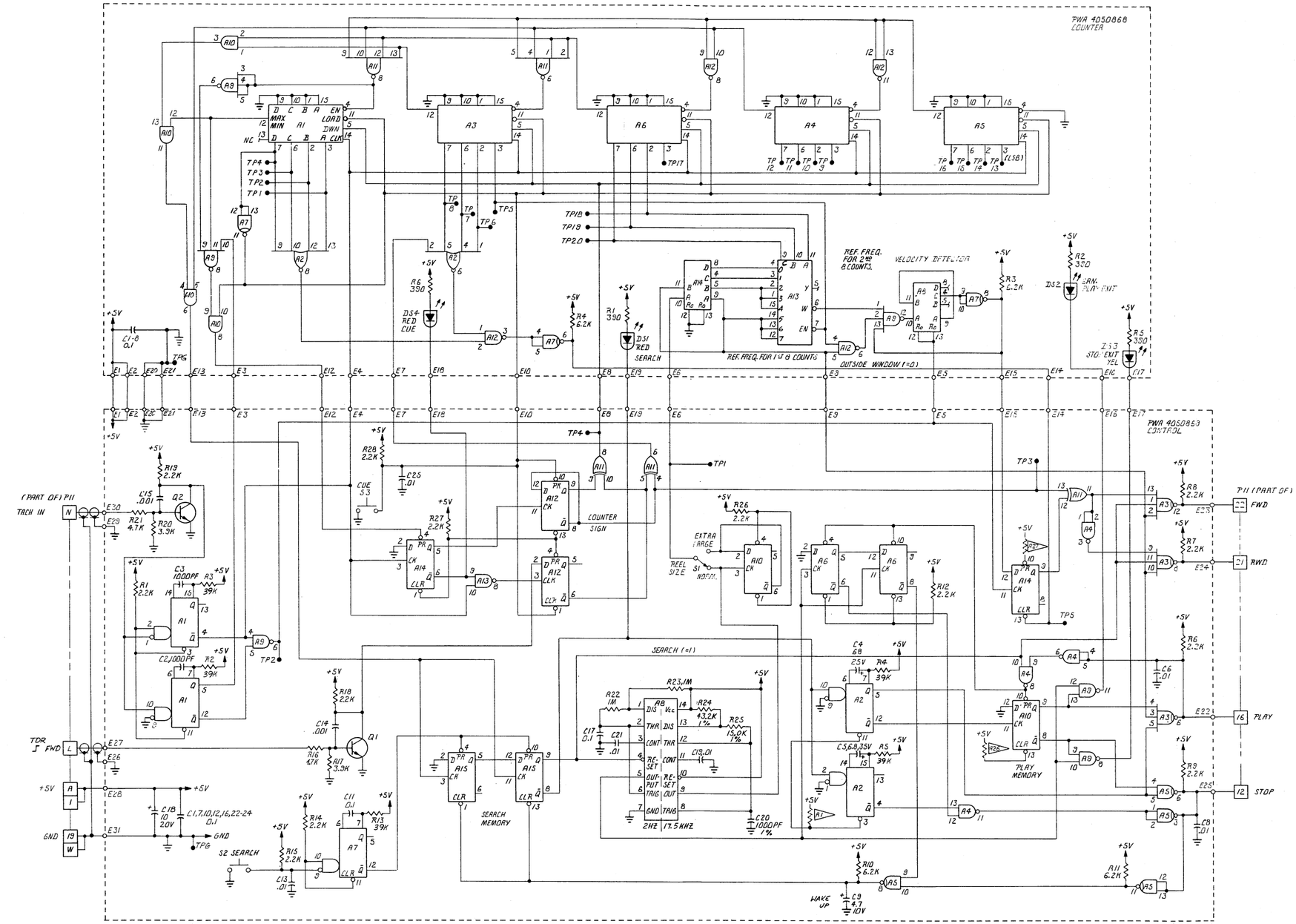
Schematic No. 4840396F.
Control Unit PWA, No. 1, 4 Channel,
No. 2, 4 Channel



Schematic No. 4840427C.
Input/Output Main Frame Assembly



Schematic No. 4840421K.
Input/Output Module PWA



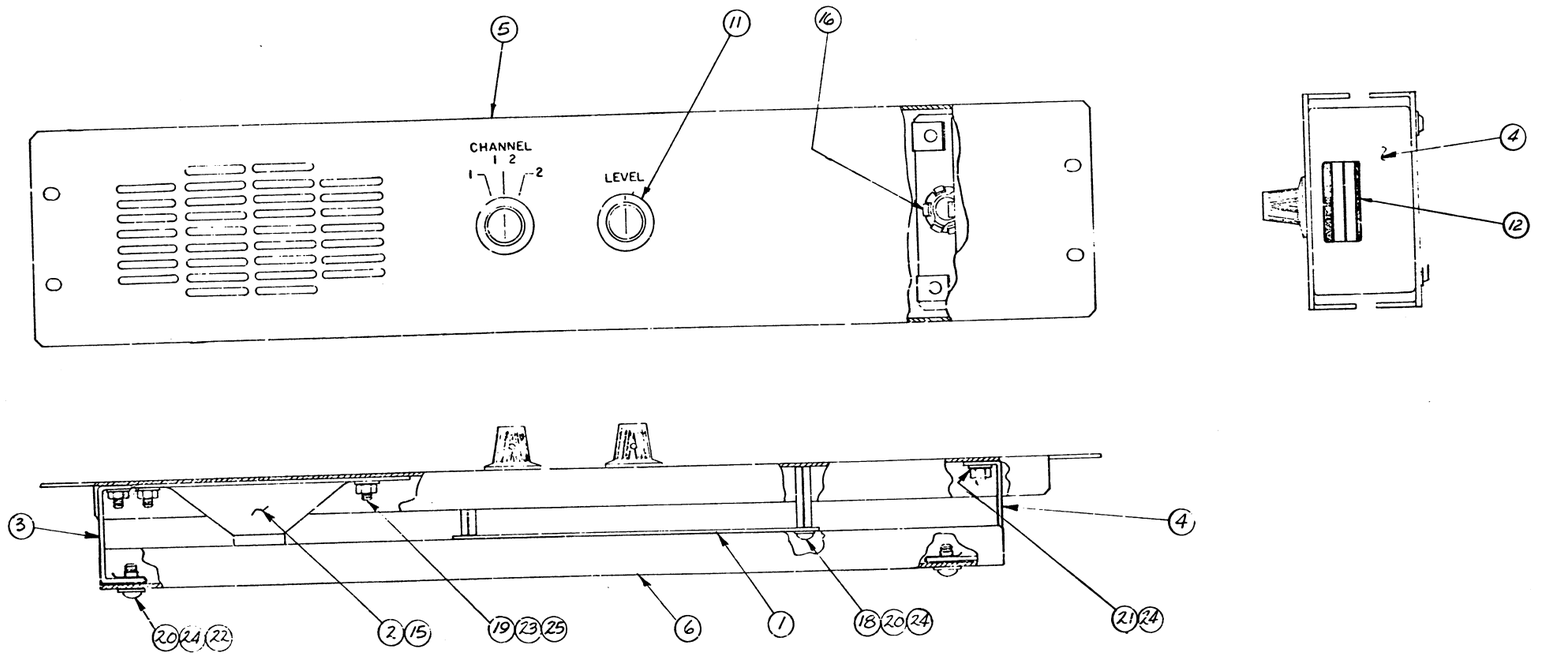
NOTES; UNLESS OTHERWISE SPECIFIED,

1. RESISTANCE VALUES ARE IN OHMS, 1/4W, 5%.
2. CAPACITANCE VALUES ARE IN MICROFARADS, 50V MIN.
3. TRANSISTORS ARE P/N 014-653, FOR FIELD SERVICE, SUBSTITUTE 2N3904.
4. PHANTOM "PULL-UP" RESISTORS R?, R28, R27 ARE SHOWN TWICE FOR CLARITY.
5. COUNTER PWA IS 4050868-01, AW IS REV 'C'.
6. CONTROL PWA IS 4050869-01, AW IS REV 'C'.

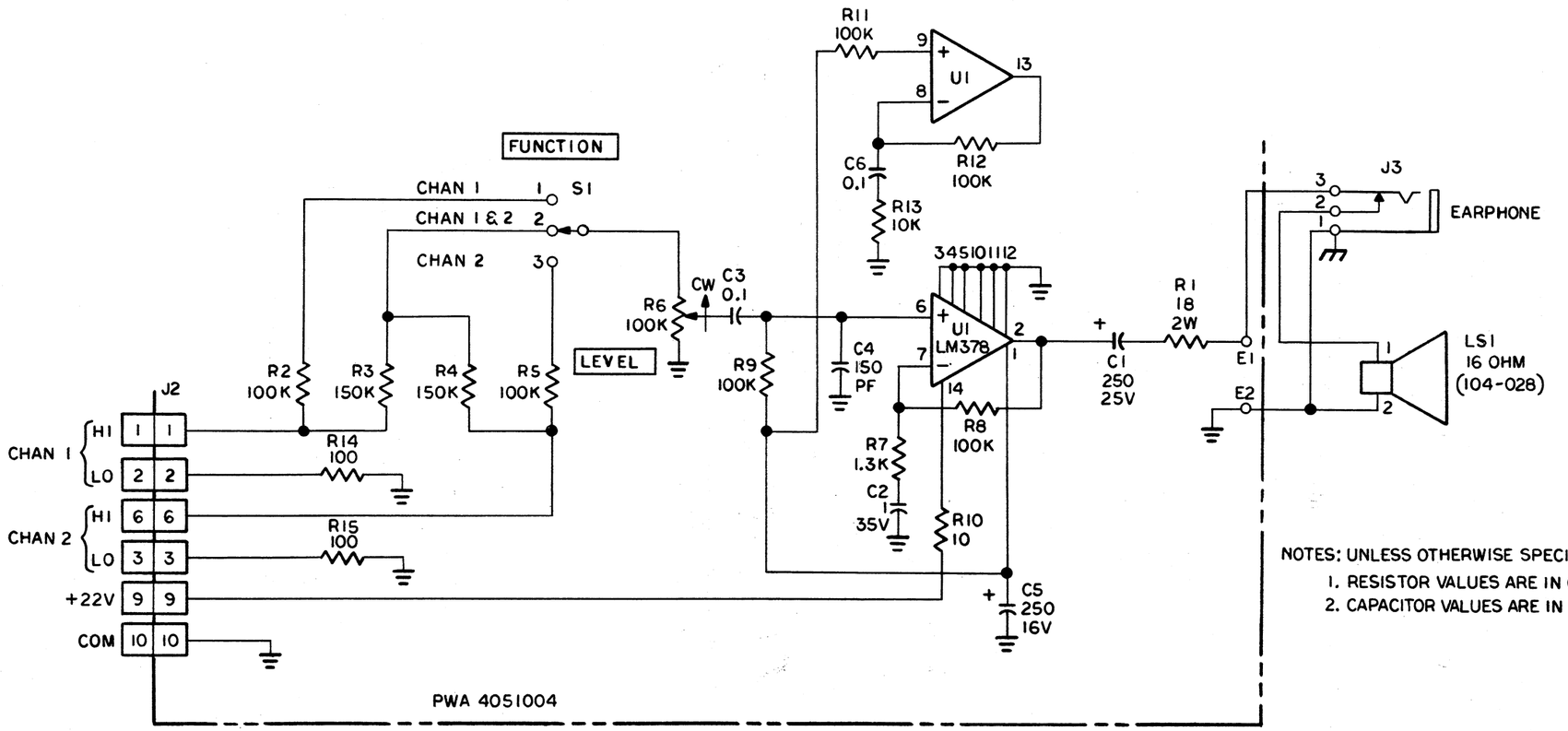
REFERENCE DESIGNATIONS			
COUNTER		CONTROL	
LAST USED	NOT USED	LAST USED	NOT USED
A-14		A-15	
C8		C25	
DS4		E31	E11
E20	E11	Q2	
R6		R28	
TP20		S3	
		TP5	

I.C. LIST										
	COUNTER						CONTROL			
REF DES	A12	A10	A9	A11	A2		A11	A5	A3	A4,9,13
AMPEX P/N	586-075	586-758	586-076	586-077	587-051		586-705	586-784	586-915	586-075
VENDOR P/N	7400	7408	7410	7420	7425		7486	7438	7412	7400
VOLTAGE PIN	14	14	14	14	14		14	14	14	14
GROUND PIN	7	7	7	7	7		7	7	7	7
REF. DES.	A7	A13	A1,3-6	A8,14			A1,2,7	A8	A6,10,12,14,15	
AMPEX P/N	586-784	586-703	587-766	589-238			587-431	589-254	586-108	
VENDOR P/N	7438	74151	74LS191	74LS293			74221	NE 556	7474	
VOLTAGE PIN	14	16	16	14			16	16	14	
GROUND PIN	7	8	8	7			8	7	7	

Schematic No. 4840439A.
Single Point Search-to-Cue Assembly



Assembly No. 4020642.
Cue Amplifier

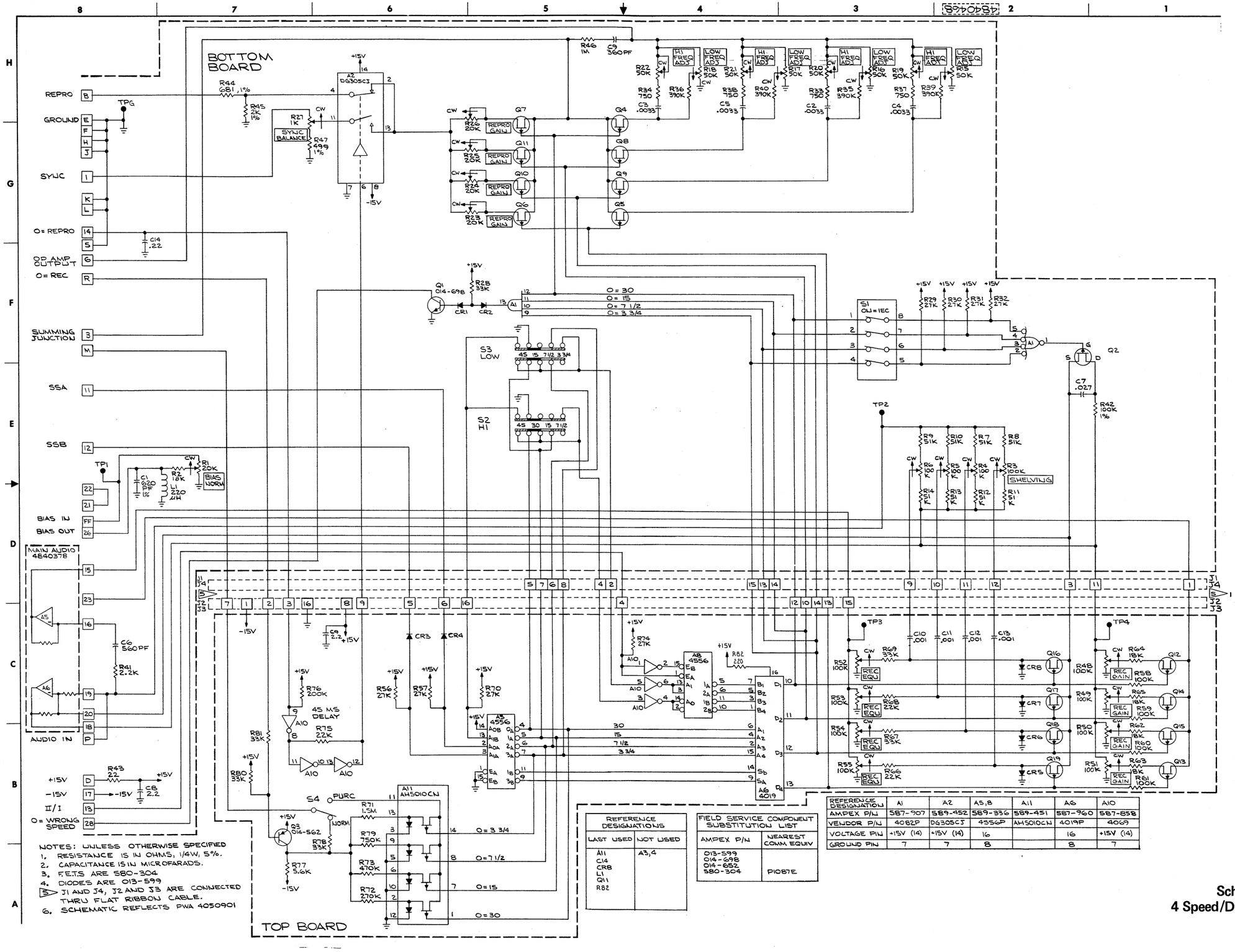


NOTES: UNLESS OTHERWISE SPECIFIED:

1. RESISTOR VALUES ARE IN OHMS, 1/4W, ±5%.
2. CAPACITOR VALUES ARE IN MICROFARADS

REF DES	
HIGHEST NO. USED	NO. NOT USED
C6 E2 J3 R13 S1 U1 LS1	J1

Schematic No. 4840516–.
Cue Amplifier PWA

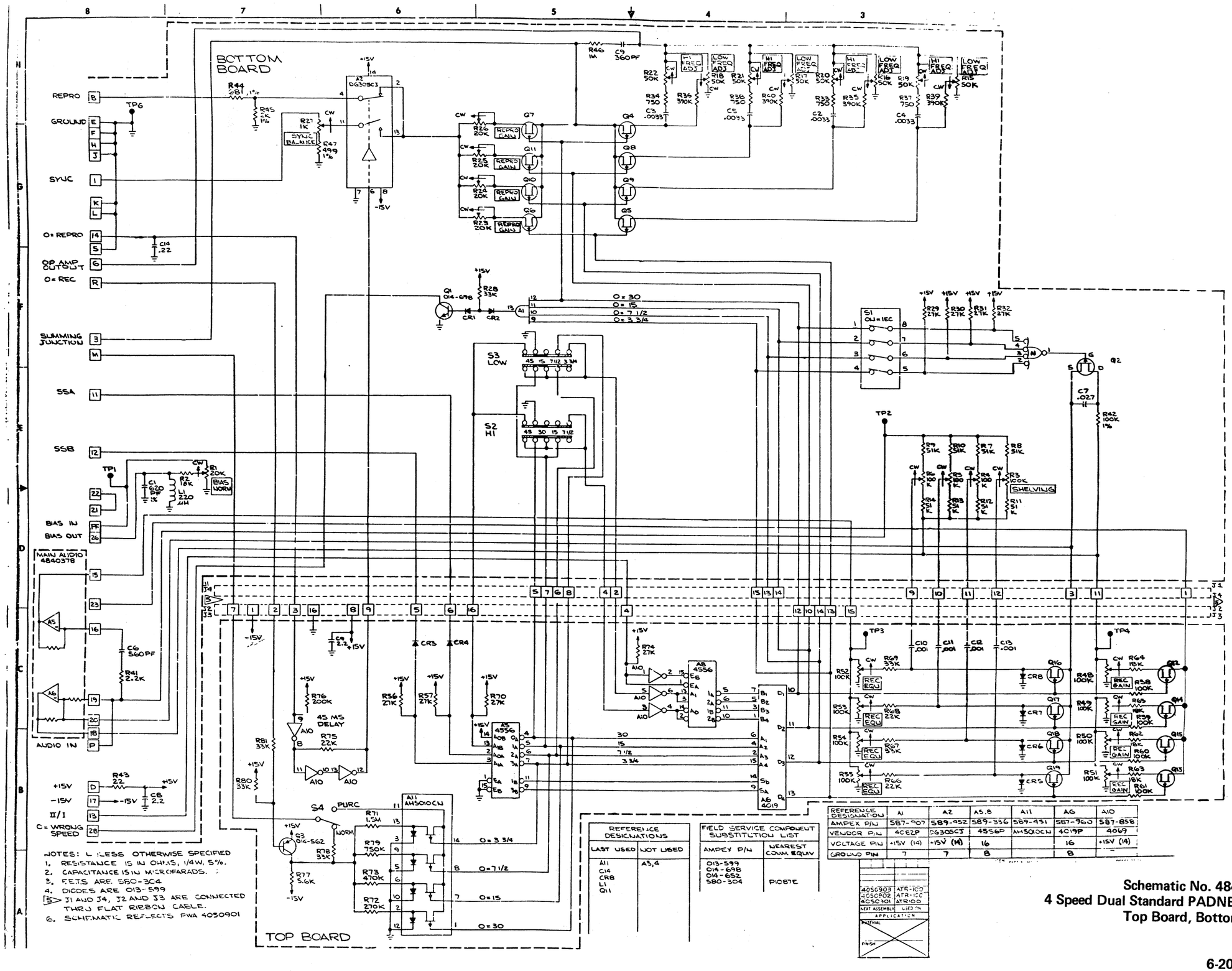


REFERENCE DESIGNATIONS	
LAST USED	NOT USED
A11	A3,4
C14	
CR8	
L1	
Q11	
R82	

FIELD SERVICE COMPONENT SUBSTITUTION LIST	
AMPEX P/N	NEAREST COMM EQUIV
013-599 014-698 014-652 580-304	P1087E

REFERENCE DESIGNATION	A1	A2	A5,8	A11	A6	A10
AMPEX P/N	587-907	589-452	589-336	589-451	587-960	587-858
VENDOR P/N	4082P	DG305CJ	4556P	AM5010CN	4019P	4069
VOLTAGE PIN	+15V (14)	+15V (14)	16		16	+15V (14)
GROUND PIN	7	7	8		8	7

Schematic No. 4840468C.
4 Speed/Dual PADNET Assembly



REFERENCE DESIGNATIONS	
LAST USED	NOT USED
A11 C14 CR8 L1 Q11	A3,4

FIELD SERVICE COMPONENT SUBSTITUTION LIST	
AMPEX P/N	NEAREST COMM EQUIV
013-599 014-698 014-652 580-304	PIO87E

REFERENCE DESIGNATION	A1	A2	A5,8	A11	A6	A10
AMPEX P/N	587-907	589-452	589-336	589-931	587-960	587-858
VENDOR P/N	4C82P	DG303CJ	4556P	AM5010CN	4C19P	4069
VOLTAGE PIN	+15V (14)	+15V (14)	16		16	+15V (14)
GROUND PIN	7	7	8		8	—

4050903	ATR-100
4050902	ATR-100
4050901	ATR100
NEXT ASSEMBLY	USED ON
APPLICATION	
MATERIAL	
FINISH	

Schematic No. 4840468B.
4 Speed Dual Standard PADNET PWA,
Top Board, Bottom Board