SECTION 4
THEORY OF OPERATION

This section of the manual provides a block diagram oriented discussion of the functional operation of the recorder/reproducer system followed by detailed theory of operation of the recorder/reproducer and input/output assembly (accessory) circuits.

4-1. FUNCTIONAL DESCRIPTION OF TAPE TRANSPORT

Figure 4-1 is a simplified block diagram of the ATR-100 system. The recorder/reproducer does not incorporate a capstan pinch roller but controls tape movement in all modes of operation while under capstan servo and reel servo control. The capstan servo controls tape speed and direction while the reel servo maintains dynamically constant tape tension in all modes of operation.

Tape movement is controlled by a dc capstan motor which is controlled by a closed loop capstan servo. The capstan is driven to control tape motion but the actual work of moving the tape is accomplished by the reel servo, which operates independent of the capstan servo. Tape tension is maintained equally on the takeup and supply side of the capstan for all sizes of tape reels (2 inches through 14 inches in diameter). Since there is no difference in tape tension at the capstan, there is no tendency for tape to slip on the capstan and therefore no pressure roller (pinch roller) is required.

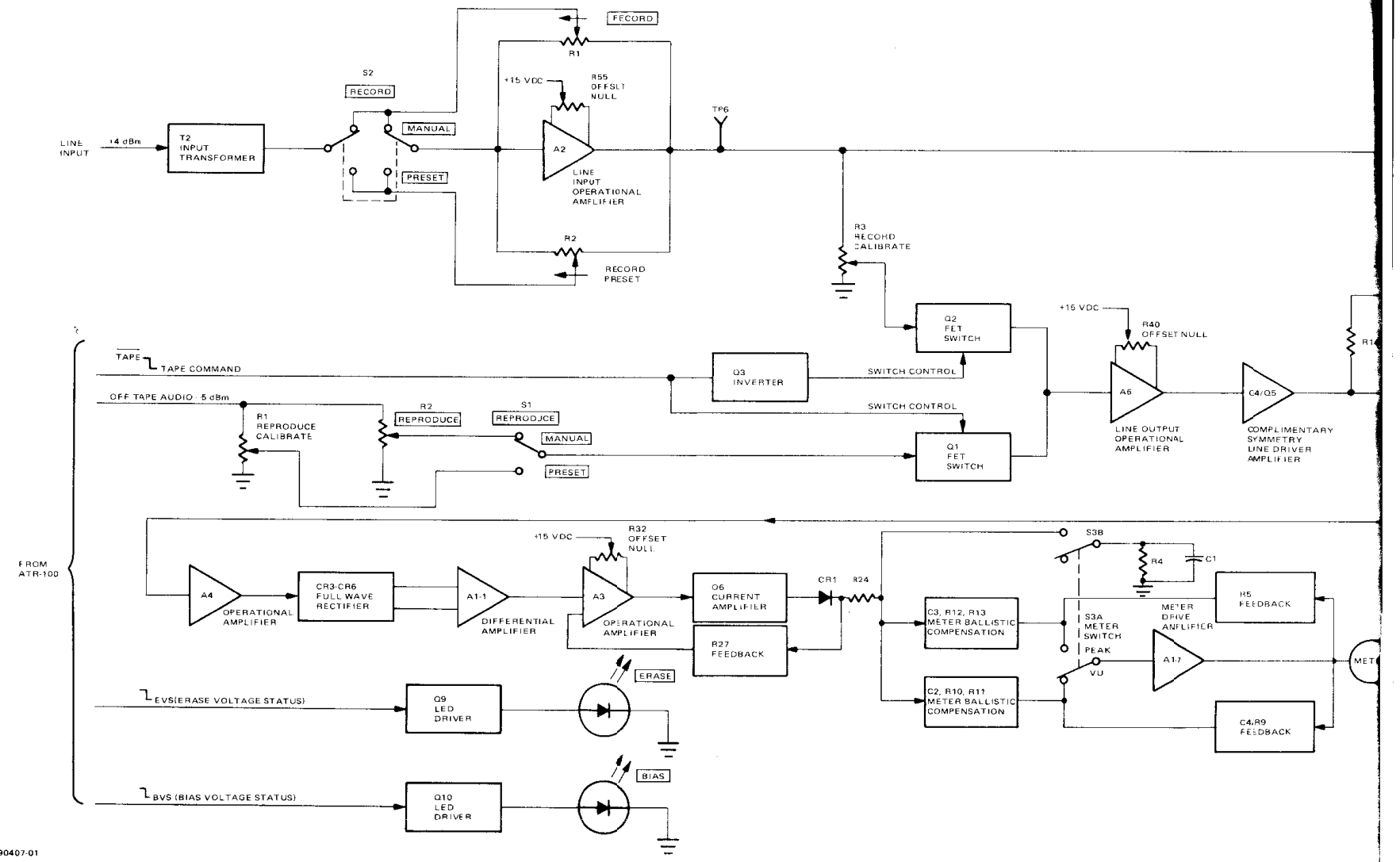
The actual value of tape tension is controlled by the tension arm rotary solenoids which are a component of the constant-tension arms. The solenoids are driven by direct current to result in a particular torque at the mid-position of the arm swing. These solenoids apply a near-constant force to the tension arms that are opposed by the force provided by the reel motors through the tape. The current in the solenoids is programmed and switched by the tension programming logic (located on reel servo PWA No. 9) depending on tape width, operating condition, and direction of tape movement to result in a given value of equal tape tension across the capstan.

The tension arms have an LED affixed to each arm and the light from the LED is focused on to a stationary photopotentiometer. The output from the photopotentiometer is a voltage indicative of arm position and is the servo error. Tape motion creates an unbalance or position error of the tension arm's position and, by means of a closed-loop reel servo, a tension unbalance is created in the tape path (but not across the capstan) by the reel motors. This tension unbalance causes the reel motors to perform the work of moving the tape at a rate established by the capstan. There are no independent commands supplied to the reel servo to cause such an unbalance. All control of the reels is initiated by capstan movement transmitted through the tape to the tension arm sensors.

The output from the tension arm sensors is amplified, compensated for the mechanical properties of the transport, and used to modulate a 28.8-kHz carrier to develop a pulse-width modulated (PWM) signal with a duty cycle that varies with the magnitude of the servo error signal. This PWM signal is amplified and used to drive the reel dc motors.

4-2. BLOCK DIAGRAM FUNCTIONAL DESCRIPTION

As shown in Figure 4-1, the ATR-100 can be configured to record and reproduce up to four audio channels. Each audio input may come from a line or other audio source, such as another tape reproducer.



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4-84. ±15-Vdc Regulator. A ±15-Vdc zener diode regulator is used to power the input/output module assembly. Power in the form of ±24 Vdc is furnished from the ATR-100 and is applied to series-pass transistors Q7 and Q8, which are connected as emitter followers. The output voltage at the emitters of Q7 and Q8 is determined by zener diodes VR1 and VR2, which are connected between the base and ground of Q7 and Q8, respectively.

4-85. Tape Timer Functional Description

The tape timer displays in hours, minutes, and seconds the elapsed time that the tape has moved at the selected speed from a zero reference established by pressing the RESET pushbutton switch on the control unit. The tape timer contains a counter and associated arithmetic logic to detect the relative tape position and provide a time-multiplexed, binary-coded decimal (BCD) output for the display of the tape position in hours, minutes, and seconds of play/record time at the selected tape speed. The tape timer receives a tape direction signal from the control unit, a selected speed signal from the tape transport, and pulses from a tape-driven tachometer (tach) on the tape transport. The tape timer counts the number of tach pulses received, converts the length of tape represented by the tach pulses to record/play time at the selected speed, and adds or subtracts the time represented by the tape motion from the current time being displayed, depending on the direction of tape motion. The tape timer sends five binary-coded decimal digits to the display on the control unit. To minimize the number of interconnecting leads between the tape timer and the control unit, the five digits are transmitted serially over a common 4-bit bus to a BCD-to-7 segment decoder in the control unit. The output of the BCD-to-7 segment decoder is sent in parallel to five 7-segment display indicators that comprise the 5-digit display on the control unit. Five digit select lines are also sent to the control unit. The digit select lines identify the current digit being sent from the tape timer and enable the corresponding one of five 7-segment display indicators.

4-86. Tape Timer Circuit Details

The tape timer circuitry is principally located on transport control PWA No. 7. The display and ancillary BCD-to-7-segment encoder are located on the control unit. Figure 4-25 is a simplified block diagram of the tape timer, and drawings 4840397 and 4840396 are the schematic diagrams, respectively.

4-87. Tape Timer Display. The tape timer display is contained on the control unit assembly and consists of five 7-segment light emitting diode (LED) display indicators (A1 through A5 on control unit PWA No. 1), five driver transistors (Q1 through Q5 on PWA No. 1), and a BCD-to-7-segment encoder (A3 on PWA No. 2). The serial stream of binary-coded decimal digits from the tape timer logic on PWA No. 7 are sent to the BCD-to-7-segment decoder A3 located on the control unit PWA No. 2. The binary-coded decimal digits are sent via 4 lines; BCD-A, BCD-B, BCD-C, BCD-D. The BCD-to-7-segment decoder A3 provides a logic low (ground) to the segments required to form the digit, which is sent in BCD via BCD-A through BCD-D, on the display.

The seven lines that comprise the output of the BCD-to-7-segment decoder A3 are sent to the control unit PWA No. 1, where they are connected in parallel to each of the corresponding segments on the five 7 segment displays, A1 through A5. Each of the five 7-segment displays consists of seven light-emitting diodes with common anodes. Selection of the 7-segment pattern corresponding to the digit sent via the BCD-A through BCD-D is accomplished by applying a positive 5 volts (logic high) to the anode of the selected 7-segment display and keeping the anodes of the other 7-segment displays at ground (logic low). The digit selection signals DS-1 through DS-5 from the tape timer circuits on the transport logic PWA No. 7, via transistor switches, provide a positive 5 volts to the anode of 7-segment display A1 through A5, respectively. When a digit select line goes low (0 Vdc), the associated transistor switch conducts and provides a positive 5 volts to the anode of the corresponding 7-segment display. Since only one digit select line goes low at a time, the remaining transistor switches are not conducting, and the

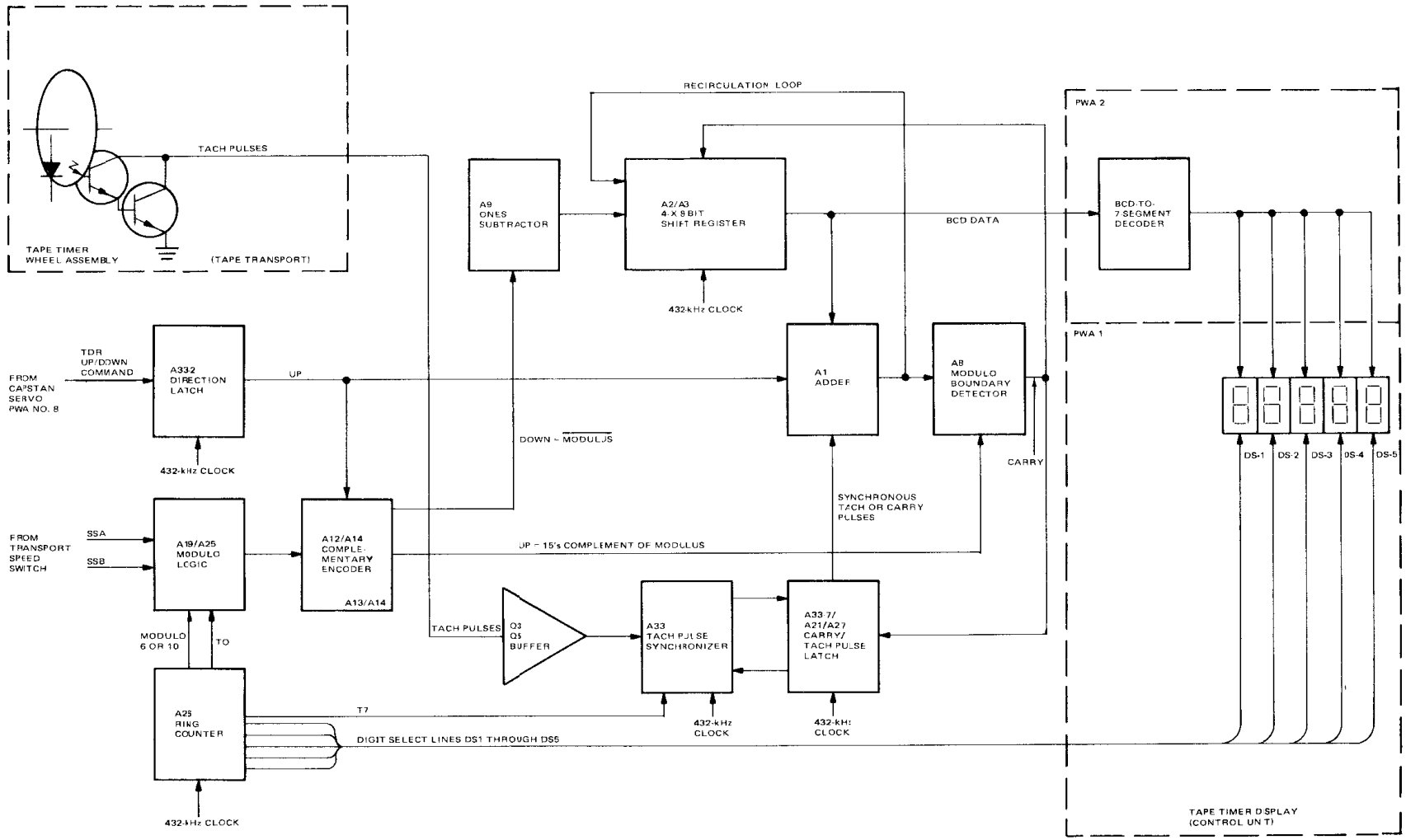


Figure 4-25. Tape Timer, Simplified Block Diagram

remaining anodes of the unselected 7-segment displays remain at 0 Vdc. Therefore, only the selected digit is lit.

4-88. Tape Timer Tachometer. The tape timer tachometer is contained on the tape transport assembly and consists of the tape wheel assembly and associated electro-optical switching assembly. The tape wheel assembly is mechanically coupled to the tape to provide one complete rotation of the tape wheel for each 7.5 inches of tape motion. The tape wheel assembly contains a shutter which interrupts the optical path of the electro-optical switch at a rate of 20 times per revolution. The electro-optical switch provides TTL-level pulses to buffer Q3-Q5 on transport control PWA No. 7. Buffer Q3-Q5 provides pulse shaping to improve the rise and fall times of the pulses received from the electro-optical switch. The buffered tachometer (tach) pulses are then sent to the tach pulse synchronizer A33-10/A33-15 that consists of two D-type latches that are clocked by the positive-going edge of the 432-kHz system clock. The tach pulse synchronizer A33-10/A33-15 retimes the tach pulses to provide a single negative-going pulse one clock period wide for each tach pulse received, regardless of the length of the tach pulse.

When the output of the buffer Q3-Q5 goes positive, latch A33-10 is set by the positive-going edge of the 432-kHz clock. The output of latch A33-10 goes to latch A33-15 and NAND gate A27-11. Latch A33-15 is set to the same state as latch A33-10 by the next positive-going edge of the 432-kHz clock. The output of latch A33-10 is combined with the complement of latch A33-15 by NAND gate A27-11 so that during the interval that latch A33-10 is first set and the time that latch A33-15 is set, one clock interval later, the output of NAND gate A27-11 goes low. During all other conditions, NAND gate A27-11 remains high. The output of NAND gate A27-11 goes to tach pulse latch A27/A21. Tach pulse latch A27/A21 is an RS-type flip-flop, which stores the received synchronous tach pulse until required by the arithmetic logic of the tape timer.

4-89. Tape Timer Arithmetic Logic. The tape timer arithmetic logic is contained on transport control PWA No. 7. The tape timer arithmetic logic consists of an up/down counter and associated control and timing logic. The up/down counter is an 8-digit serial binary adder that circulates data through a 4-bit parallel adder serially by digit. The up/down counter provides the incrementing and decrementing of time in hours, minutes, and seconds and division of the tach pulse rate according to the selected operating speed. An 8-bit ring counter identifies the digit currently at the output of the 8-digit, 4-bit, serial binary adder and provides the control for multiplexing the digits from the adder at the control unit display. The operations within the tape timer arithmetic logic are synchronized by the 432-kHz clock. Table 4-8 shows the format for the eight 4-bit digits contained in the four 8-bit shift registers and the time interval during which each of the 4 bits representing a single digit are available at the output of the register.

As shown in Table 4-8, the first time period (t_0) contains a digit whose modulus varies with the tape speed. Since the tach pulses are generated at a rate of 20 times per 7.5 inches of tape, the modulus of the digit at time t_0 varies with the tape speed selected to divide the tach pulses by a factor which provides 10 pulses per second at the selected operating speed. At a selected operating speed of 30, 15, 7.5, and 3.75 inches per second, the modulus of the digit at t_0 is 8, 4, 2, and 1, respectively. The digits at time t_1 through t_7 represent the operating time in hours, minutes, seconds, and tenths of a second at the selected operating time. Only five digits are displayed on the control unit.

Table 4-8. Counter Data Word Format

MODULO	TIME
Tape-Speed Divider (modulo depends on tape speed selected)	t_0
Tenths of Seconds (modulo 10)	t_1
Units of Seconds (modulo 10)	t_2
Tens of Seconds (modulo 6)	t_3
Units of Minutes (modulo 10)	t_4
Tens of Minutes (modulo 6)	t_5
Units of Hours (modulo 10)	t_6
Tens of Hours (modulo 10)	t_7

The digits at time t_1 through t_5 or at time t_2 through t_6 may be selected by link strapping on the tape timer logic assembly to display tenths of a second, seconds, and minutes or to display seconds, minutes, and hours, respectively, on the control unit display. The output signals from the ring counter are strapped to the enable signal lines, DS-1 through DS-5, to select the appropriate digit on the control unit display.

The tape up/down counter in the tape timer logic consists of shift register A2/A3, adder A1, ones subtractor A9, modulo boundary detector A8, and carry flip-flop A33-7. The up/down counter shifts each digit in the counter data word in a 4-bit slice to the data output lines. If a tach pulse is not received by the tape timer logic within the previous cycle (t_0 through t_7), the data is recirculated through the up/down counter without being modified. If a tach pulse is received by the tape timer logic during the previous cycle (t_0 through t_7), the count in the up/down counter is incremented by one when the tape motion is in a forward direction, or decremented by one when the tape motion is in the reverse direction.

The timing and control logic of the tape timer consists of ring counter A26, direction latch A33-2, modulo logic A19/A25, complementary encoder A13/A14, and tach pulse latch A21/A27. Ring counter A26 is clocked by the positive-going edge of the 432-kHz signal and generates the 8-bit time intervals (t_0 to t_7) for one cycle of operation of the up/down counter. The modulo logic A19/A25 receives the speed selector signals, SSA and SSB, from the tape transport speed selector switch and timing information from the ring counter A26. The modulo logic generates the 15's complement of the modulus for each digit in the counter data word at the corresponding time interval. The modulo information, in 15's complement form, is sent to complementary encoder A13/A14. Complementary encoder A13/A14 provides the modulus or its complement to ones subtractor A9 or modulo boundary detector A8, respectively. Direction latch A33-2, which is set by the tape up/down command TDR, generates the control signal UP to complementary encoder A13/A14. The UP signal, if set (high), gates the complemented modulus to modulo boundary detector A8. If the UP signal is reset (low), the modulus is sent to subtractor A9. The UP signal is also sent to adder A1 where it provides the control signal to increment or decrement the counter when a tach pulse has been received.

The modulo information is sent to the complementary encoder A13/A14 which provides the modulus or its complement to the ones subtractor A9 or the modulo boundary detector A8, respectively. Tape direction latch A33-2, which is set by the tape up/down command (TDR), generates the control signal (UP) to the complementary encoder A13/A14. The UP signal, if set (high), gates the 4-bit complement of the modulus to modulo boundary detector A8. If the UP signal is reset (low), the modulus is sent to the ones subtractor A9 in BCD. The UP signal is also sent to adder A1 where it provides the control signal to increment or decrement the counter when a tach pulse has been received.

4-90. Initialization. The tape timer is initialized by pressing and releasing the RESET pushbutton on the control unit. Pressing the RESET pushbutton generates a low CRB signal to the tape timer. When CRB is low, the tach and carry pulses from the carry flip-flop A33-7 are inhibited from going to the counter and the contents of 4-by-8-bit shift register A2/A3 are cleared. The tape timer is also initialized by the wakeup signal, which is generated when power is first applied to the unit, via a "wired-OR" that forces the CRB line to the tape timer logic low.

4-91. Count-Up Mode. When the tape is moving forward, the tape timer is in a count-up mode. During this time, the TDR signal (up/down command) is high. When the TDR signal is high, direction latch A33-2 is set by the positive-going edge of the 432-kHz clock. With direction latch A33-2 set, the output of the carry flip-flop A33-7 is directed to the carry input of adder A1 through NOR gate A20-1; the 4-bit data from the modulo logic is gated to modulo boundary detector A8 via the complementary encoder A13/A14; and the 4-bit data to the ones subtractor A9 is low. Figure 4-26 shows a simplified block diagram of the serial adder formed by 4-by-8-bit shift register A2/A3 and associated components A1, A8, and A9.

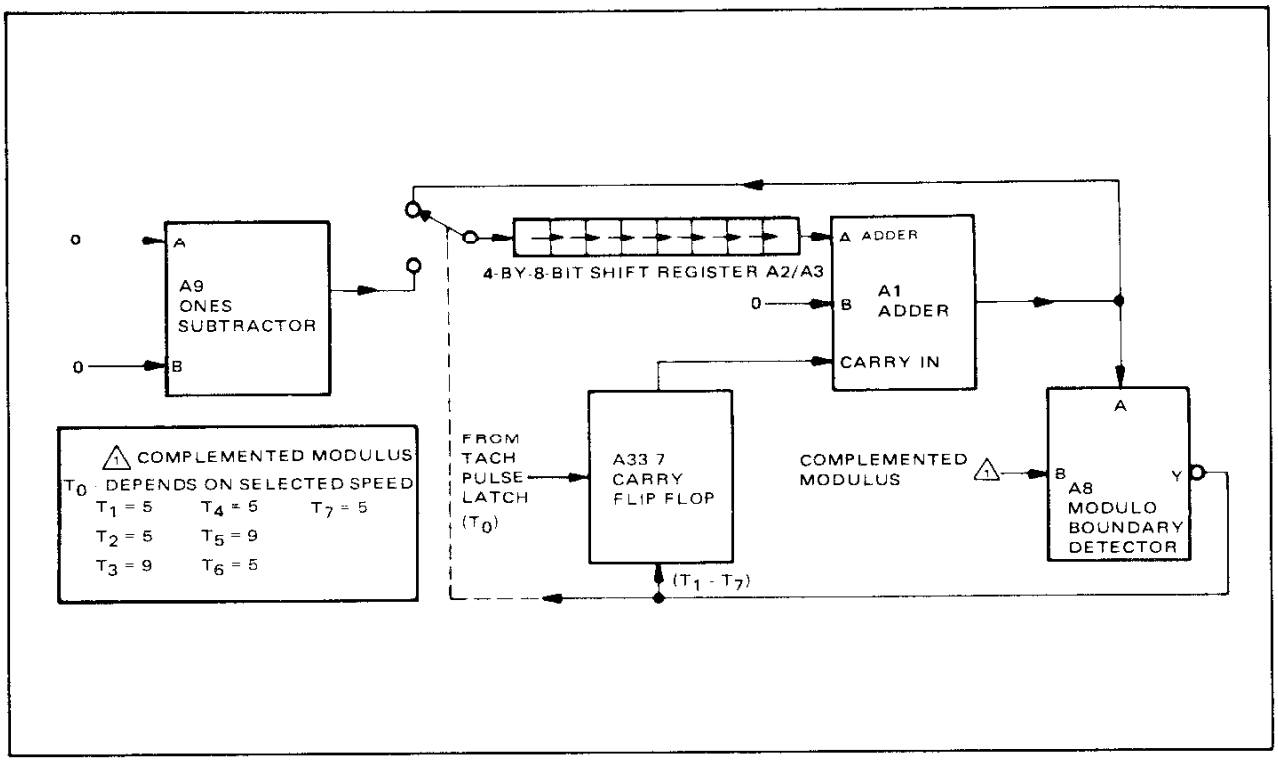


Figure 4-26. Count Up Logic, Simplified Block Diagram

As shown in Figure 4-26, each BCD digit is shifted through the shift register and adders as a parallel 4-bit number. The data through 4-by-8-bit shift register A2/A3 is shifted serially by the 432-kHz signal. At time t_0, the least significant bit of the eight-digit BCD number is shifted out of the register to the A inputs of adder A1. During the count-up mode, the B inputs to adder A1 from NOR gate A20-13 are low, and the carry in to adder A1 will go high only when a tach pulse had been received during the previous t_0 through t_7 cycle, or a carry is generated at any other period than t_7. If no tach pulse was received during the previous cycle (t_0 through t_7), the least significant digit which is present at t_0 will be unchanged by adder A1. The output of adder A1 is recirculated back to the input of 4-by-8-bit shift register A2/A3. The output of the adder A1 is also sent to the A input of modulo boundary detector A8. The B input to modulo boundary detector A8 is the 15's complement of the modulus for that specific digit. At time t_0, the modulus is determined by the setting of the speed selector on the tape transport. The complemented modulus at the B input to modulo boundary detector A8 during t_0 will be 7, 11, 13, and 14 for selected speeds of 30, 15, 7.5, and 3.75 inches per second, respectively.

The output of adder A8 goes to NAND gate A31-6, which provides a low (0 Vdc) signal to the data selection input of the shift register and, via NAND gate A27-6, to carry flip-flop A33-7. As long as no tach pulses are received by the tape timer logic, the count continues to be recirculated through the shift register unchanged and the output of NAND gate A31-6 remains high. When a tach pulse is received at the end of t_7, the carry flip-flop A33-7 is set, which generates an input to adder A1 during t_0. This input increments the least significant digit from the shift register. The incremented output of adder A1 is summed with the complemented modulus by modulo boundary detector A8. If the resulting sum does not equal 15, NAND gate A31-6 remains high. With NAND gate A31-6 high,

the incremented digit is clocked back into the shift register at the start of t_1 and the carry flip-flop A33-7 is not set again. Therefore, the remaining digits at t_1 through t_7 will be recirculated unchanged through the shift register. If at the start of t_0, a tach pulse had been received and the resulting incremented output of adder A1 plus the complemented modulus equaled 15, the output of NAND gate A31-6 would go low. With the output of A31-6 low, the incremented digit is not recirculated back to the shift register. Instead the output of the ones subtractor A9 is selected. During count up, the output of ones subtractor A9 is always equal to 0.

In addition to selecting the output of ones subtractor A9 as the input of the shift register, the low output of NAND gate A31-6, via NAND gate A27-6, sets carry flip-flop A33-7 at the start of the next time interval (t_1). At t_1, the second least significant digit is shifted out to adder A1 and, if carry flip-flop A33-7 is set (least significant digit + complemented modulus = 15), the carry in to adder A1 is high and the second least significant bit will be incremented. The sum from adder A1 during time t_1 is added to the complemented (base 16) modulus by modulo boundary detector A8 and, if the sum equals 15, NAND gate A31-6 goes low. If NAND gate A31-6 goes low, zero is loaded into the shift register and the carry flip-flop A33-7 is set to provide a carry in to adder A1 at t_2. If the sum out of modulo boundary detector A8 did not equal 15, NAND gate A31-6 will remain high and the incremented sum out of adder A1 is recirculated back to the shift register. This process repeats during each successive bit time, t_2 through t_6. At t_7, the most significant digit is shifted out of 4-by-8-bit shift register A2/A3 to adder A1. The status of the carry flip-flop A33-7 is inhibited from generating a carry in to adder A1 by the t_7 timing pulse via buffer A37-12, which is "wire-ANDed" with the output of carry flip-flop A33-7 via buffer A37-10. Since during t_7 the most significant digit is never incremented, a carry is not generated into the least significant digit as a result of the most significant digit exceeding the modulus.

4-92. Count-Down Mode. When the tape is moving in a reverse direction, the tape timer is in a count-down mode. During this time, the TDR signal (up/down command) is low. When the TDR signal is low, direction latch A33-2 is reset by the positive-going edge of the 432-kHz signal. When direction latch A33-2 is reset, the output of carry flip-flop A33-7 is directed to the B inputs of adder A1 through NOR gate A20-13, the 4-bit data from the modulo logic is gated to ones subtractor A9 via complementary encoder A13/A14, and the 4-bit B input to modulo boundary detector A8 is low. Figure 4-27 shows a simplified block diagram of the serial adder formed by 4-by-8-bit shift register A2/A3 and associated logic components A1, A8, and A9.

As shown in Figure 4-27, each BCD digit is shifted through the shift register and logic as a parallel 4-bit number. The data through 4-by-8-bit shift register A2/A3 is shifted serially by the 432-kHz signal. At time t_0, the least significant digit of the eight-digit BCD number is shifted out of the register to the A inputs of adder A1. During the count-down mode, the carry in to adder A1 from NOR gate A20-1 is held low, and the 4-bit B inputs to adder A1 will go high when a tach pulse has been received during the previous t_0 through t_7 cycle or a carry is generated at any other period than at t_7. If not tach pulse is received during the previous cycle (t_0 through t_7), the least significant digit which is present at t_0 will be unchanged by adder A1. The output of adder A1 is recirculated back to the input of 4-by-8-bit shift register A2/A3. The output of adder A1 is also sent to the A input of the modulo boundary detector A8. The B input to modulo boundary detector A8 will always be 0 during the count-down mode. Ones subtractor A9 is used to input the data into shift register A2/A3 when a borrow is detected. The A input to ones subtractor A9 is the modulus for that specific digit. During time t_0, the modulus at the A input to ones subtractor A9 will be 8, 4, 2, or 1 for selected tape speeds of 30, 15, 7.5, and 3.75 inches per second, respectively. All four B inputs will always be high during count down thereby adding 15 (or the sixteens complement of one). Therefore, during count down, the sum output of the ones subtractor A9 will always be equal to the modulus minus 1. This ensures that the correct number is present to succeed zero in the count-down sequence.

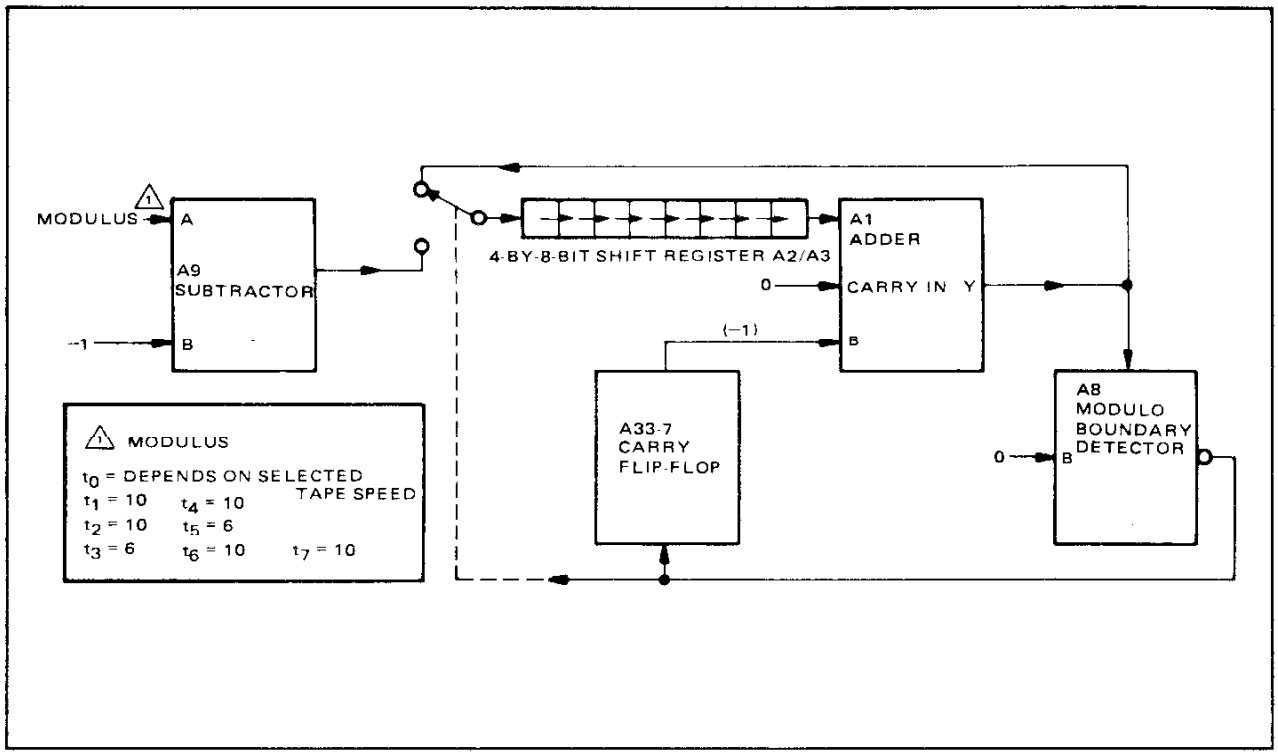


Figure 4-27. Count Down Logic, Simplified Block Diagram

When a tach pulse has been received during the previous cycle (t_0 through t_7), carry flip-flop A33-7 is set at start of t_0. The set output from carry flip-flop A33-7 is gated to the B inputs of adder A1 via NOR gate A20-13; therefore, when the carry flip-flop is set, all B inputs will be high. When the carry flip-flop A33-7 is reset, all B inputs will be low. At time t_0, the least significant digit is shifted out of shift register A2/A3 to adder A1. If a tach pulse was not received, the sum output of adder A1 will be recirculated to the input of shift register A2/A3 unchanged. If a tach pulse was received in the previous cycle, carry flip-flop A33-7 is set at t_0 and the least significant digit that is being shifted out at this time is summed with the B input to adder A1, which is all ones. By adding all ones (or the sixteens complement of one) to the output of the shift register, one is subtracted from the count. The sum from adder A1 is sent to modulus boundary detector A8 where it is transferred to the inputs of NAND gate A31-6 unchanged since, during count down, only 0 (all B inputs low) is added to the sum from adder A1 by A8. If decrementing the least significant digit generates a 15 (0 minus 1 equals 15 in hexadecimal), NAND gate A31-6 goes low and sets carry flip-flop A33-7 at the end of t_0.

At the same time that NAND gate A31-6 goes low, the output of ones subtractor A9 is substituted for that of adder A1 at the input of 4-by-8-bit shift register A2/A3. This output is always equal to one less than the modulus of the digit currently being processed. At t_1, the second least significant digit is transferred out of shift register A2/A3 to adder A1. If at t_0 the carry flip-flop A33-7 was set, the second least significant bit will be decremented. The output of adder A1 is checked by modulo boundary detector A8 in the same manner as during t_0 for a count of 15. If the count of 15 is not detected, the output of the adder is recirculated back to 4-by-8 shift register A2/A3.

If 15 (15 equals zero count) is detected as the result of decrementing the digit from the shift register, the output of ones subtractor A9 is shifted into 4-by-8-bit shift register A2/A3 as the correct number to follow zero in the count-down sequence. In a similar manner, the remaining digits, t_2 through t_7, are processed in the count-down mode with the exception that during t_7 the output of the carry flip-flop A33-7 is disabled.

4-93. Tape Run Out. If the tape runs out, tach pulses may still be generated by the tachometer wheel due to inertia. In order to prevent the tach pulses from being counted, an abort signal, generated by the tape transport when the tape runs out, inhibits the output from carry flip-flop A33-7. The abort signal is received by open-collector buffer A37-8. The output of open-collector buffer A37-8 is "wired-ORed" with buffer A37-10, which buffers the output of the carry flip-flop A33-7. When the abort signal goes low, the buffered output of the carry flip-flop A33-7 is held low by buffer A37-8 and further counting of tach pulses is inhibited.

4-94. Power Supply Functional Description

The power supply assembly, with the exception of three transport mounted transistors, filter capacitors, rectifiers, and transformer, is contained on a single PWA. Main ac power is connected to the ATR-100 through a captive 3-wire power cable attached to the power supply bracket. Power is applied to the primary windings of the transformer via the POWER ON/OFF switch which is mechanically linked to the transport assembly. A jumper plug arrangement in the primary of the power transformer allows selection of any one of four input voltage ranges of 50 or 60 Hertz primary power to be used with the ATR-100. The primary power input voltages that can be accommodated by this arrangement are: 90 to 115 Vac, 110 to 135 Vac, 180 to 230 Vac, and 220 to 270 Vac. The power supply assembly provides unregulated ±20 Vdc (nominal) for use by the reel and capstan servo motors, electronically filtered ±20 Vdc (nominal) for use by the audio circuits, and regulated +5 Vdc for use by the TTL circuits. Additionally, the power supply assembly also contains the current sense resistors for the reel motors and the dynamic braking circuits to stop the reel motors in the event of loss of power or control.

4-95. Power Supply Circuit Details

The power supply assembly is a separate self-contained assembly with the exception of three series-pass transistors located on the transport assembly. Figure 4-28 is a simplified block diagram of the power supply assembly and drawing number 4840412 is the schematic diagram.

4-96. AC Supply. As shown in Figure 4-28, the main ac power to the power supply assembly is supplied to transformer T1 via fuse F1 and switch S1. Taps from transformer T1 to the switched main ac power are accessible via a jumper plug arrangement on the power supply assembly to allow the use of one of four input voltage ranges to be selected as the input to transformer T1 and to provide 115 Vac to the transport. The secondary of transformer T1 consists of three windings. One winding provides ac input to the 5-Vdc regulated supply. The other two windings provide the ac input to the 20-volt electronically filtered supply and 20-volt servo supply.

4-97. 20 Volt Servo Supply. The 20-volt servo supply consists of a rectifier and isolation network which provide the +20 Vdc and −20 Vdc to the reel-motor and capstan servos. Unregulated 20-Vdc rectifier A2 consists of a bridge rectifier assembly and two filter capacitors. The bridge rectifier assembly is connected to the secondary windings of transformer T1 to act as two full-wave rectifiers, one for the +20 Vdc and the other for the −20 Vdc. A filter capacitor at the output of each full-wave rectifier filters the +20 Vdc and 20 Vdc. The filtered +20 Vdc and −20 Vdc is supplied to the capstan motor via an isolation network consisting of diodes CR3/CR4 and filter capacitors C6/C7.

4-98. 20-Volt Electronically Filtered Supply. The 20-volt electronically filtered supply consists of 20-volt rectifier A1, +20-Vdc floating reference capacitor C2, −20-Vdc floating reference capacitor C4, overcurrent shutdown transistors Q1/Q3/Q4/Q6, +20-Vdc driver Q2, −20-Vdc driver Q5, +20-Vdc series-pass transistor Q8, and −20-Vdc series-pass transistor Q9. (These transistors are located

on the transport heatsink.) The 20-volt electronically filtered supply provides +20 Vdc and −20 Vdc (22 Vdc, nominal) for use by the audio circuits. The 20-volt rectifier A1 is a bridge rectifier assembly connected to the secondary winding of transformer T1 to act as two full-wave rectifiers; one rectifier to provide the +20 Vdc and the other rectifier to provide the −20 Vdc. The outputs of 20-volt rectifier A1 provide the +20-Vdc and −20-Vdc floating references via capacitor C2 and driver Q2 for the +20-Vdc and via capacitor C4 and driver Q5 for the −20 Vdc. Drivers Q2 and Q5 provide the electronically filtered +20 Vdc and −20 Vdc to the +20-Vdc series-pass transistor Q8 and −20-Vdc series-pass transistor Q9, respectively. Overcurrent shutdown transistors Q1/Q3/Q4/Q6 provide dual shutdown of the +20-Vdc and −20-Vdc outputs when excessive current is drawn from either output. If excessive current is drawn from either +20-Vdc or −20-Vdc output, overcurrent shutdown transistors Q1/Q3/Q4/Q6 will cause both outputs to go to 0 Vdc and remain at 0 Vdc until power is removed for approximately 10 seconds and reapplied. Transistors Q1 and Q4 and resistors R2 and R10 provide current sensing for the +20-Vdc and −20-Vdc outputs, respectively. The output at the collectors of Q1 and Q4 go to the bases of each other and to the bases of transistors Q3 and Q6, which shunt the floating references to drivers Q2 and Q5 and cause the outputs to go to 0 Vdc for both +20 Vdc and −20 Vdc.

4-99. 5-Vdc Regulated Supply. The 5-Vdc regulated supply consists of +5-Vdc rectifier CR1/CR2, +5-Vdc reference Q7/VR3, +5-Vdc driver Q8, +5-Vdc series-pass transistor Q10, and crowbar Q11. Additionally, reel servo interlock and dynamic brake K1/Q9/Q10 are operated from the 5-Vdc regulated supply. The 5-Vdc regulated supply provides the +5 Vdc to the TTL circuits on the ATR-100. The reel servo interlock and dynamic braking provides dynamic braking of the takeup and supply motors in the event of power failure or loss of reel servo control.

The +5-Vdc rectifier CR1/CR2 consists of a full-wave rectifier and associated filter capacitor. The rectified +5 Vdc goes to +5-Vdc reference Q7/VR3 and +5-Vdc series-pass transistor Q10, via a 3 ampere fuse (F2). The +5-Vdc reference Q7/VR3 consists of current source Q7 and reference diode VR3. Current source Q7 provides a constant current to reference diode VR3. The reference voltage from reference diode VR3 is supplied to the base of driver Q8, which is connected to +5-Vdc series-pass transistor Q10 in a darlington configuration. Series-pass transistor Q10 provides the current required by the TTL circuits at the reference voltage minus the voltage drop across the base-to-emitter drop of Q8 and Q10. Part of output from +5-Vdc series-pass transistor Q10 is sampled by crowbar Q11 via 5.6V zener diode VR4. When the voltage at the output of series-pass transistor Q10 rises above +5.6V plus the trip voltage required to trigger SCR Q11, the current through zener diode VR4 rises and provides the gate current to SCR Q11 in crowbar Q11/VR4. SCR Q11 is connected across the +5-Vdc input, to series pass transistor Q10, and ground. When SCR Q11 conducts, the +5-Vdc input to series-pass transistor Q10 is shunted to ground causing fuse F2 to open.

Reel servo interlock and dynamic brake K1/Q9/Q10 contains relay driver Q9/Q10, double-pole double-throw relay K1, full-wave rectifier CR9/CR10, and motor loads DS1/R25 and DS2/R26. Reel servo interlock and dynamic brake K1/Q9/Q10 disconnects the output of supply motor MDA and takeup motor MDA from the supply and takeup motors, respectively, and connects the motor loads to the motor to provide dynamic braking when reel servo on (SVO) goes high or +5 Vdc is lost.

Full-wave rectifier CR9/CR10 provides +24 Vdc from transformer T1 to the high side of relay coil K1. The return for relay coil K1 is provided by relay driver Q9/Q10. When SVO is low (0 Vdc) and +5 Vdc is present at the output of the 5-Vdc regulated supply, relay driver Q9/Q10 provides a return path and energizes relay coil K1. When K1 is energized, the supply motor MDA is connected to the supply motor and the takeup motor MDA is connected to the takeup motor. If SVO goes high or +5 Vdc is lost, K1 is de-energized. When K1 is de-energized, the takeup motor is switched from the takeup motor MDA to motor load DS1/R25 and the supply motor is switched from the supply motor MDA to motor load DS2/R26. Motor loads DS1/R25 and DS2/R26 provide a path for the current generated by the back emf of the motor

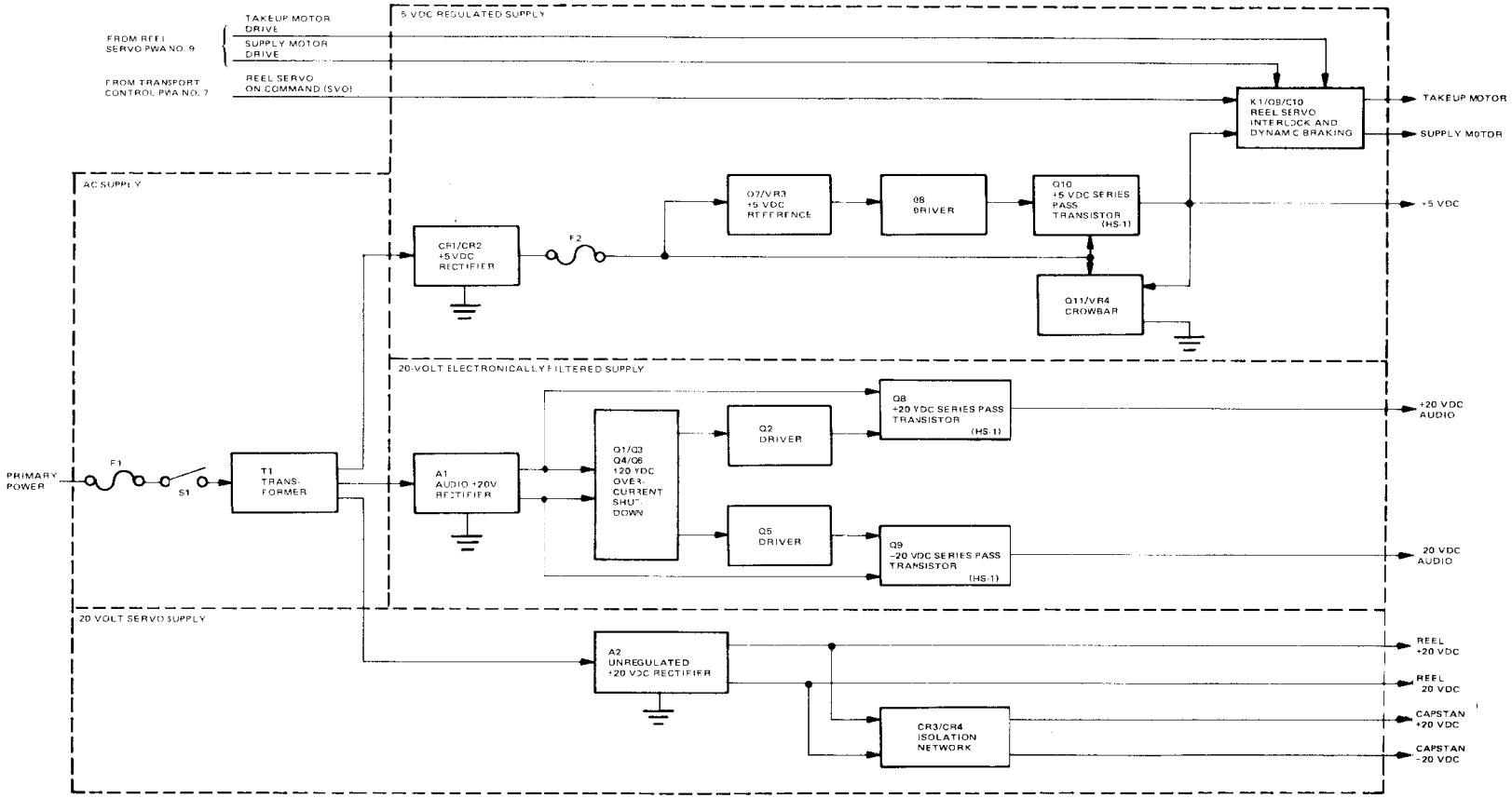


Figure 4-28. Power Supply Assembly, Simplified Block Diagram

4-3. Thread Mode

When power is applied and tape is threaded and taut so that either tape taut switch is closed, pressing the stop pushbutton switch enables the transport control PWA No. 7 logic circuitry to activate the reel servos (reel servo PWA No. 9) and place system into thread mode. After thread mode is established, any other mode may be entered.

4-4. Reproduce Mode

When play mode (or record mode) is selected, the capstan motor is initially driven by a fixed dc current source until a phase-lock condition is achieved, and then the motor is controlled by the output of a phase comparator (capstan servo PWA No. 8). The inputs to the phase comparator are a submultiple of a 9.6-kHz reference frequency (submultiple frequency used depends on selected tape speed) and the capstan tachometer pulses from the capstan motor assembly. As discussed in paragraph 4-1, tape movement is sensed by the supply and takeup sensors on the constant-tension arms and causes the reel servos (reel servo PWA No. 8) to control tape-reel movement.

The audio signal recovered from the tape by the record (Sel-Sync operation) or reproduce head(s) is amplified and equalized on the audio and PADNET PWA(s) and routed to the audio output for external processing, or to the optional input/output assembly for further amplification.

4-5. Record Mode

In the record mode, tape is moved across the heads under reel servo and capstan servo control as in play mode. During record mode, an erase signal (144 kHz) and bias signal (432 kHz) from the master oscillator on audio control PWA No. 5 are fed to the audio and PADNET PWA(s). The erase signal is fed to the erase head(s) to erase any previously-recorded signals from the tape before it reaches the record head(s). Information to be recorded is amplified, added to the bias signal, and applied to the record head(s). The information is recorded on the tape as it passes over the record head. However, actual recording on tape is not permitted to begin until the capstan servo is phase locked and a command signal is routed from the capstan servo (PWA No. 8) via transport control (PWA No. 7) and audio control (PWA No. 5) to the main audio PWA(s). After actual recording on tape has begun, bias and erase status signals are routed to the input/output assembly to cause the BIAS and ERASE confidence indicators to illuminate.

4-6. Spool Mode

In spool mode, capstan and reel servo operation is identical to play and record mode operation except the reference frequency furnished to the phase comparator (capstan servo PWA No. 8) from the audio control PWA No. 5 is either 9.6 kHz for 60-in/s operation, or 28.8 kHz for 180-in/s operation. In spool mode, circuitry on reel servo PWA No. 9 and transport control PWA No. 7 causes the tape lifter solenoid to be energized and lift the tape from the heads.

4-7. Shuttle Modes

In fast forward or rewind modes, the capstan is driven by a dc current driver (capstan servo PWA No. 8) rather than the phase comparator circuit. As in play, record, and spool modes, the tape movement is sensed by the supply and takeup sensors on the constant tension arms and, by means of the closed-loop reel servo, tape is moved from reel to reel.

4-8. Control Unit

The control unit is used to initiate all transport and signal mode functions by means of pushbutton switches which control mode latching circuits on transport control PWA No. 7 and on audio control PWA No. 5, respectively. The control unit also houses LED indicators that indicate system modes of operation. The LED indicators associated with signal mode selection are driven by multiplexer circuitry on audio control PWA No. 5.

The play, stop, record, fast forward, rewind, and edit indicators are driven by logic circuitry on transport control PWA No. 7. These indicator drives are not multiplexed.

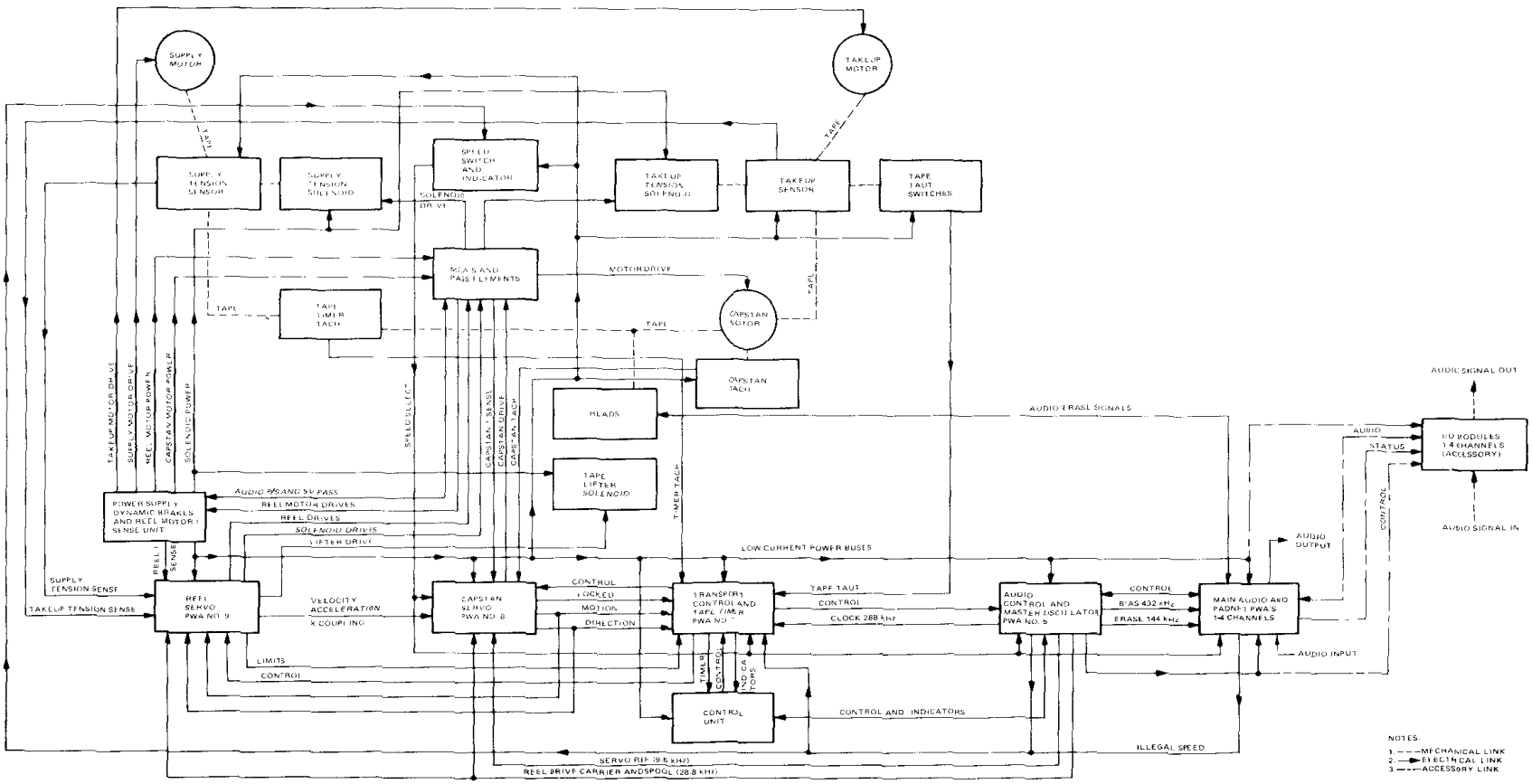


Figure 4-1. ATR-100 System, Simplified Block Diagram

Also located on the control unit is the tape timer display which consists of five 7-segment LED display indicators. The transport tape timer tachometer furnishes pulses when tape is in motion to the tape timer circuitry on transport control PWA No. 7. Timer display information, in the form of a serial stream of binary-coded decimal digits, is sent to a decoder in the control unit. Digit select signals are also routed from transport control PWA No. 7 to the control unit in order to select the digit for display in the proper sequence on the tape timer LED display.

4-9. DETAILED THEORY OF OPERATION

Detailed theory of operation of the recorder/reproducer and input/output assembly (accessory) is presented in the text that follows. Simplified functional block diagrams support the text as an aid in understanding the ATR-100 circuitry. For the complete schematic diagrams, see Section 6 of this manual.

Logic elements are identified in the text and block diagrams by their schematic reference designator and output pin number. For example, A3-1 refers to integrated circuit A3, output pin number 1. In the case where there is more than one output pin, the true (high) or active output pin designation is used.

Logic level commands used throughout the system are designated on the schematics and block diagrams by their three-letter abbreviation. All commands are a logic low, except for the LFT command and where complimentary logic is required. For example, the ready/safe command is so identified in the text but is designated ready¬safe on the block diagrams. This indicates the ready command is a logic high and the safe command is a logic low. Table 4-1 is an *alphabetical list (by* abbreviation) of all commands used throughout the system.

Table 4-1. Command Signal Abbreviation

ABBREVIATION	COMMAND
BCD – A – D	Binary-coded decimal drive to 7-segment decoder

Table 4-1. Command Signal Abbreviation (Continued)

ABBREVIATION	COMMAND
BCS	Bias command status
BVS	Bias voltage status
CLK	Clock
CRB	Counter reset button
CS1 – 4	*Channel* select buttons
DRC	Command direction
DS1 – 5	Digit select lines
EDB	Edit button
EDI	Edit indicator
ERS	Electronics record status
EVS	Erase voltage status
FFB	Fast forward button
FFI	Fast forward indicator
ILM	Inner limit
IPB	Input button
ISL	Illegal speed lockout
LFT	Tape lift command
LKD	Locked
MRB	Main record bus
MTS	Motion sense
OLM	Outer limit
PDR	Play and record
PEC	Play edit command
PLB	Play button
PLC	Play command
PLI	Play indicator
RCB	Record button
RCI	Record indicator
RDB	Ready button
RED	Remote edit
RPB	Reproduce button
RWB	Rewind button
RWI	Rewind indicator
SFB	Safe button
SHC	Shuttle command
SPC	Spool command
SSA	Speed select A
SSB	Speed select B
STB	Stop button
STC	Stop command
STI	Stop indicator
STP	Stop pulse
SVO	Servos on command
SYB	Sync button
TDR	True direction
TLM	Torque limit
TTS	Tape taut switch
WUL	Wake-up line

4-10. Capstan Servo
Functional Description

The capstan servo is a closed-loop type of servo that controls the speed and direction of the dc capstan motor during all recorder modes of operation. Figure 4-2 is a general block diagram of the capstan servo system. During operation, tachometer pulses are generated at a rate proportional to speed. These pulses are amplified, shaped, and fed as one input to a digital phase comparator. The other input to the phase comparator is a reference signal. This reference signal is derived from a master oscillator and determines the record, play, and spool speeds of the recorder. When the phase comparator is locked to the two signals, a rectangular-wave error signal is provided by the phase comparator. This signal is fed through a carrier filter and a compensation amplifier to a motor drive amplifier (MDA) that drives the dc capstan motor.

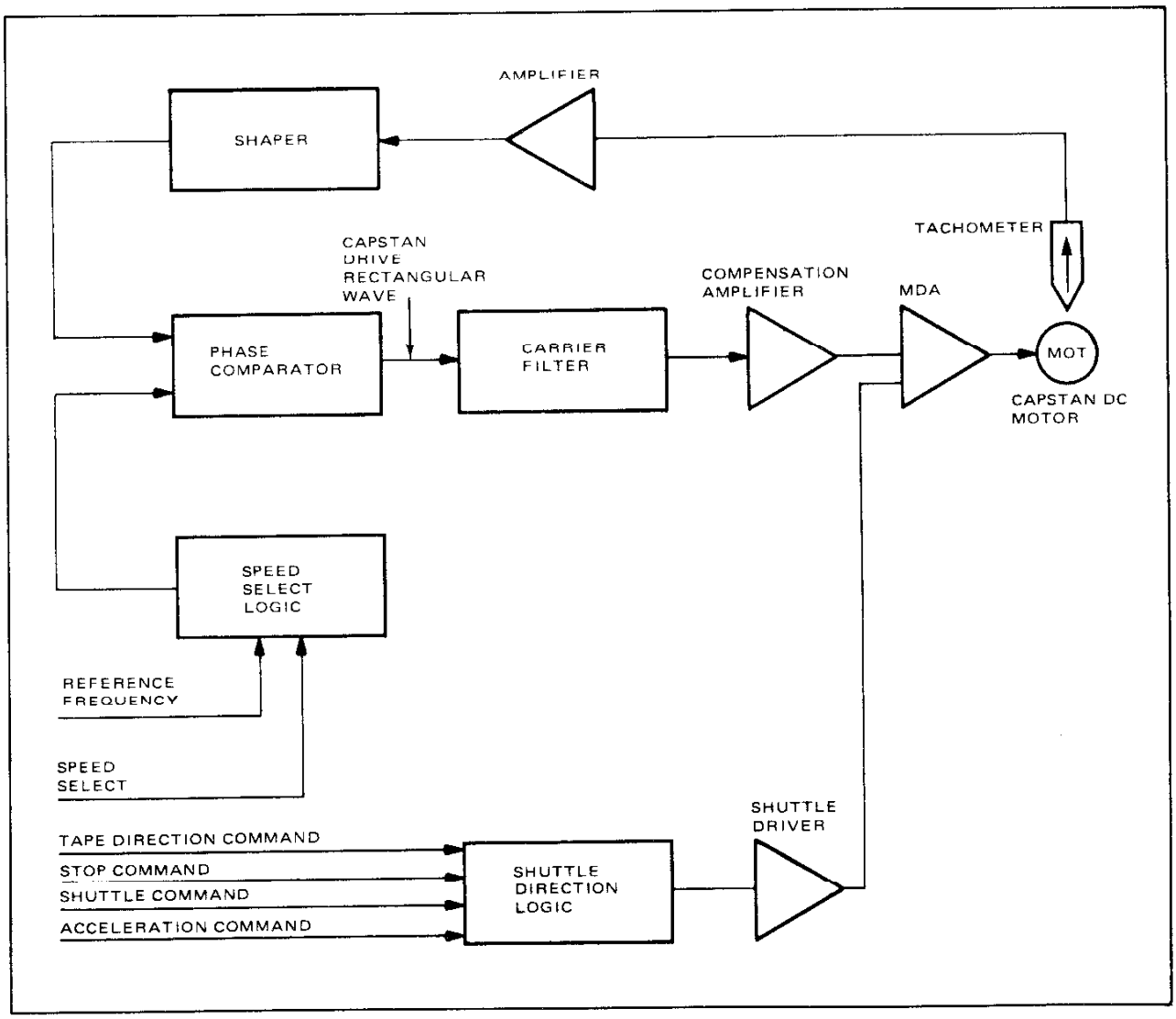
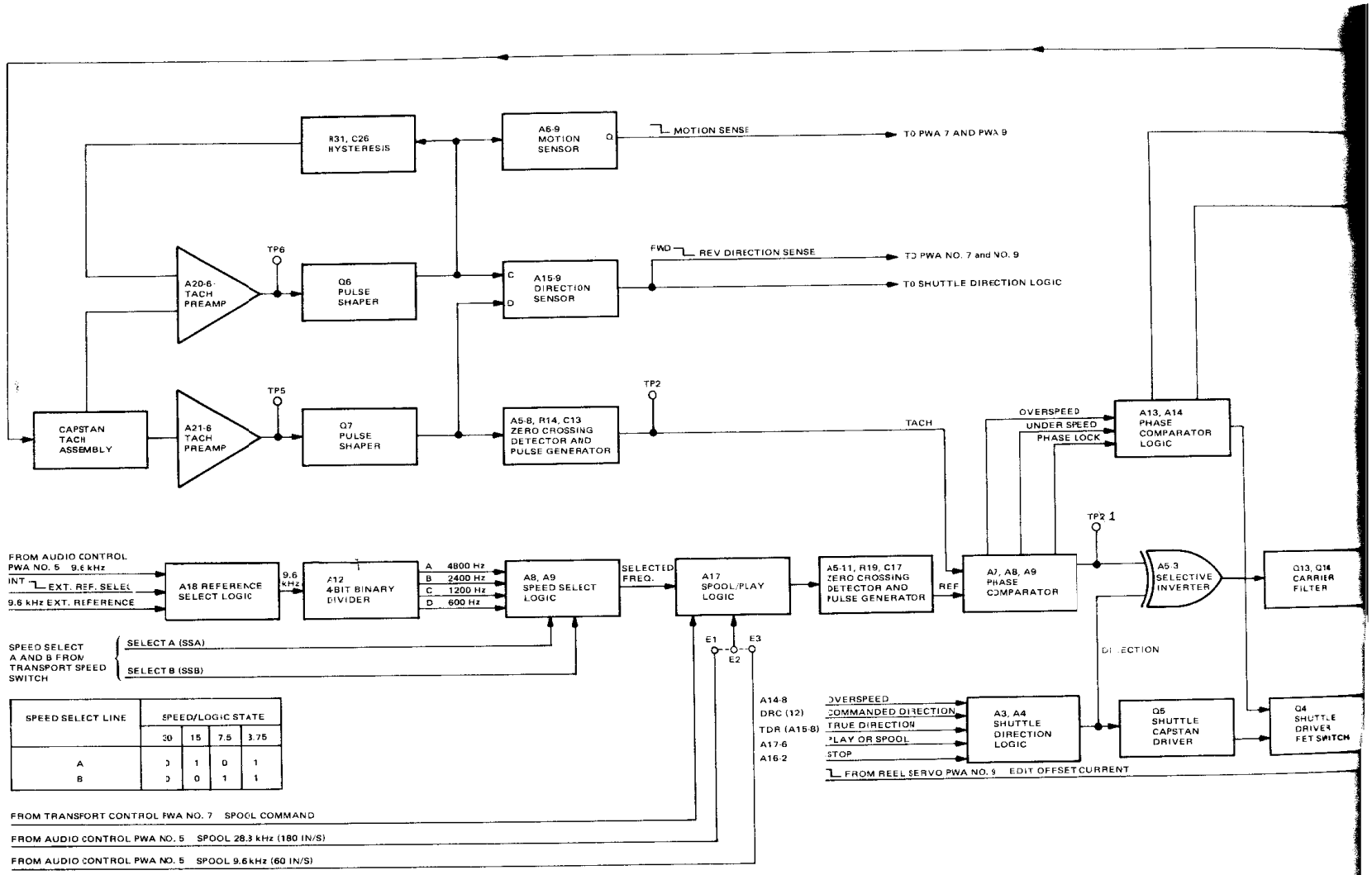


Figure 4-2. Capstan Servo General Simplified Block Diagram



SPEED SELECT LINE	SPEED/LOGIC STATE			
	30	15	7.5	3.75
A	0	1	0	1
B	0	0	1	1

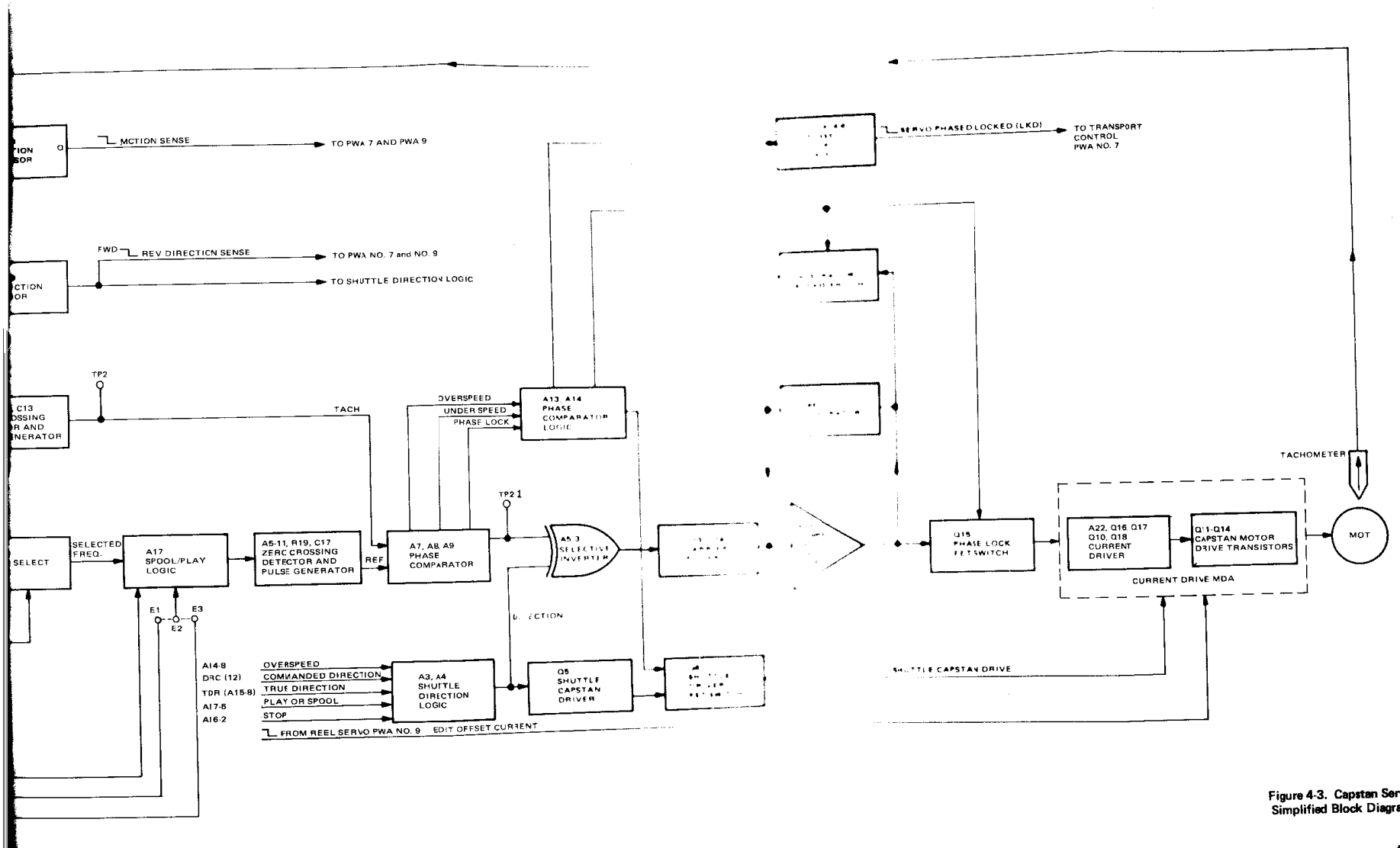


Figure 4-3. Capstan Servo Simplified Block Diagram

Table 4-2. Phase Comparator Output Logic States

GATE	SERVO CONDITION		
	UNDERSPEED	OVERSPEED	PHASE LOCKED
A9-6	H	L	H
A7-11	L	H	H
A14-8	L	H	L
A14-11	H	L	H
A13-6	H	H	L
A14-3	H	L	L
A13-12	H	L	L

Table 4-3. Tape Speed Reference Frequencies

TAPE SPEED (IN/S)	MODE	REFERENCE FREQUENCY
180	Spool	28.8 kHz
60	Spool	9,600 Hz
30	Play/Record	4,800 Hz
15	Play/Record	2,400 Hz
7.5	Play/Record	1,200 Hz
3.75	Play/Record	600 Hz

As shown on simplified block diagram Figure 4-3, a 9,600-Hz reference signal from audio control PWA No. 5 or an external source is applied to the reference select logic A18. A command signal routed from accessory connector J11 selects either the internal or external reference signal, and the selected signal is applied to the clock input of 4-bit binary, divider A12. When play or record mode is selected, the divider is enabled by a low applied to its reset inputs. The 9,600-Hz signal is divided down (4,800 Hz, 2,400 Hz, 1,200 Hz, and 600 Hz) and applied to the play/record speed select logic (A10/A11-8). The speed select signal, in the form of a 2-bit binary encoded signal from the transport speed select switch is applied to the input of the speed select logic A10/A11. The speed select logic permits the selected frequency to pass to the spool/play-record select logic (A17). When in play or record mode, gate A17-8 is enabled and passes the selected frequency to zero crossing detector and pulse generator A5-11/R19/C17. The generator provides a 1-μs positive-going pulse for each transition of the reference square-wave signal. These pulses are applied as the reference signal for the phase comparator.

For selection of spool speed, a jumper on PWA No. 8 is positioned to select 60 or 180 in/s (during recorder installation). These speeds correspond to a reference frequency of 9,600 Hz or 28.8 kHz respectively. When spool mode is selected, a low command signal is applied to the spool/play-record select logic (A17) to lockout the play/record frequencies and enable the preselected (jumper) spool frequency. The enabled spool frequency is applied to the zero crossing detector and pulse generator as in play/record modes.

4-15. Direction Logic and MDA Driver. Direction logic A3/A4 accepts input signals from five sources and determines what the polarity of the capstan motor drive voltage should be for the various recorder modes of operation. These input signals are from the phase comparator logic A13/A14; direction sensor A15-9; and the spool, play, and shuttle direction commands from transport control PWA No. 7. The output of the shuttle direction logic (A4-11) is a logic high for forward direction and a logic low for reverse direction. For shuttle modes, for initiation of play or record mode before phase lock is achieved (underspeed condition), and for capstan drive to stop, the level from A4-11 is inverted by A19-6 and applied to shuttle driver Q5 which translates the logic level to +5 Vdc for a forward direction motor rotation and −5 Vdc for reverse direction motor rotation. This voltage level is routed through FET switch Q4, which is enabled by the phase detector logic, to the capstan MDA to drive the capstan motor.

It should be noted that these voltage levels do not necessarily result in the capstan turning in the particular direction of the drive signal, but are sometimes used to stop rotation. For example, when fast forward mode is in operation and a stop command is given, the drive signal polarity is reversed to stop the capstan rotation.

For play, record, or spool modes of operation, the output of the direction logic (A4-11) is applied to EXCLUSIVE OR-gate A5-3 to control the polarity of the rectangular wave output from the phase detector.

4-16. Capstan Motor Edit Offset. In stop/edit mode of operation, power is removed from the takeup reel and the tension arm roller is pressed against the capstan. To prevent the supply reel holdback tension from pulling the capstan backwards when capstan drive power is removed, a current is sourced into the capstan MDA summing node (pin 6 or A22-7). A low play/edit command (PEC) from transport control PWA No. 7 is inverted by A14-2 on reel servo PWA No. 9 and is routed through R124 as an edit-offset current to the capstan MDA on capstan servo PWA No. 8.

4-17. Play Mode. When play (or record) mode is selected, the capstan motor is initially driven by the shuttle driver (underspeed condition) until phase lock is achieved. After phase lock is achieved, control of the motor is switched to the output of the phase comparator. (See *Direction Logic and MDA Driver*, paragraph 4-15.)

4-18. Underspeed Condition. To prevent motor overshoot when the servo switches to phase-lock control, the compensation amplifier integrator capacitor (C49) is disabled by shunt switch Q11 during motor acceleration. A logic high from the phase detector logic (A14-3) turns Q11 on during the underspeed condition. Also the phase detector logic provides a high (A14-3) to turn FET switch Q15 off, and a high (A13-12) to turn FET switch Q4 on. When Q15 is off, the compensation amplifier output is disconnected from the MDA, and when Q4 is on the capstan motor is driven by shuttle capstan driver Q5. The on/off state of the FET switches is summarized in Table 4-4.

4-19. Phase Lock. When phase lock is achieved, the phase detector logic turns Q4 and Q11 off, and turns Q15 on. Then the MDA drive signal path is from the phase detector through EXCLUSIVE OR gate A5-3, carrier filter Q13/Q14, compensation amplifier A22-1, to the capstan MDA.

Table 4-4. Capstan Servo FET Switch Control

SERVO CONDITION	INTEGRATOR BYPASS SWITCH Q11	PHASE LOCK SWITCH Q15	SHUTTLE DRIVER SWITCH Q4
UNDERSPEED	ON	OFF	ON
OVERSPEED	OFF	ON	OFF
PHASE LOCKED	OFF	ON	OFF
STOPPED	OFF	OFF	OFF

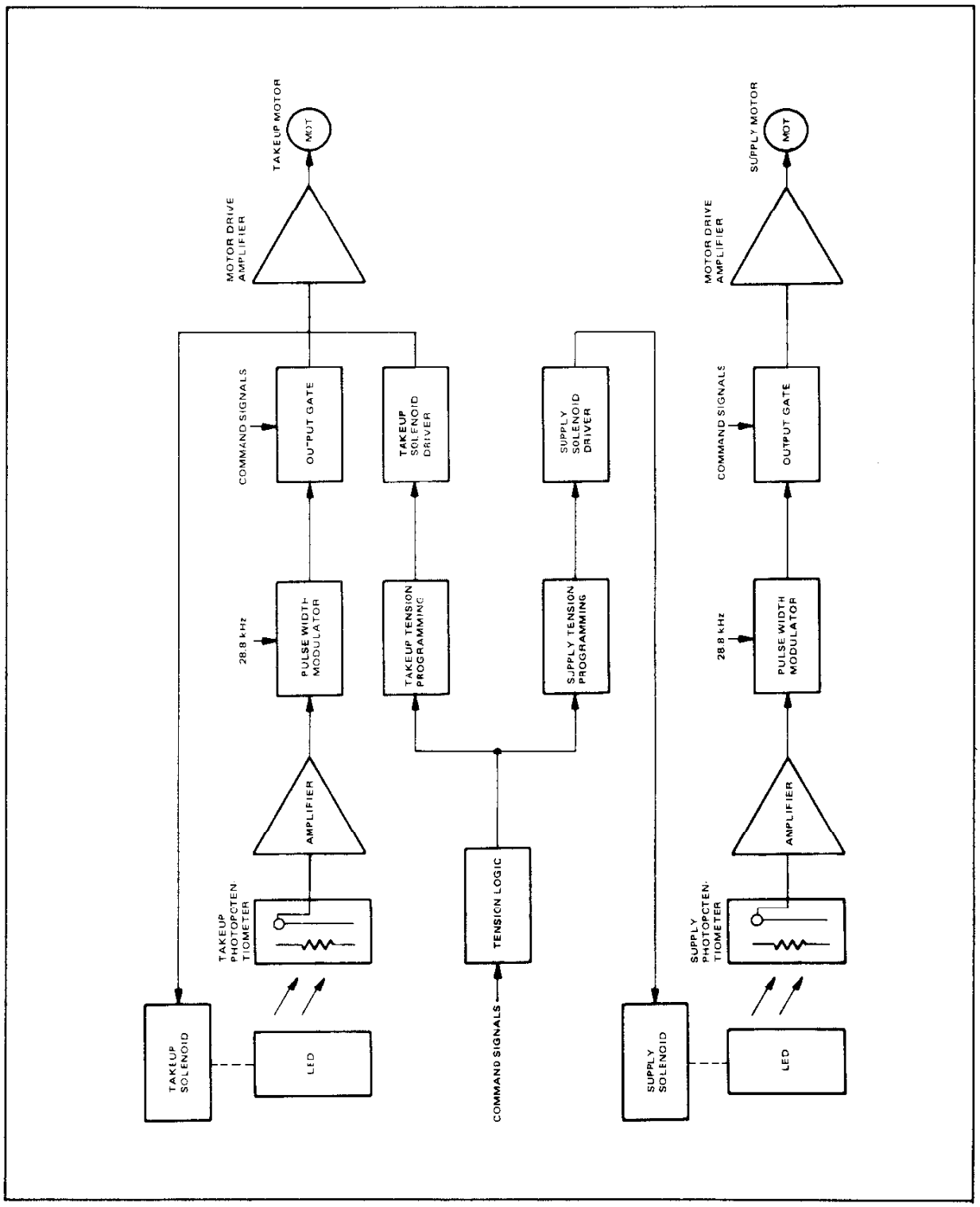


Figure 4-4. Reel Servo General Simplified Block Diagram

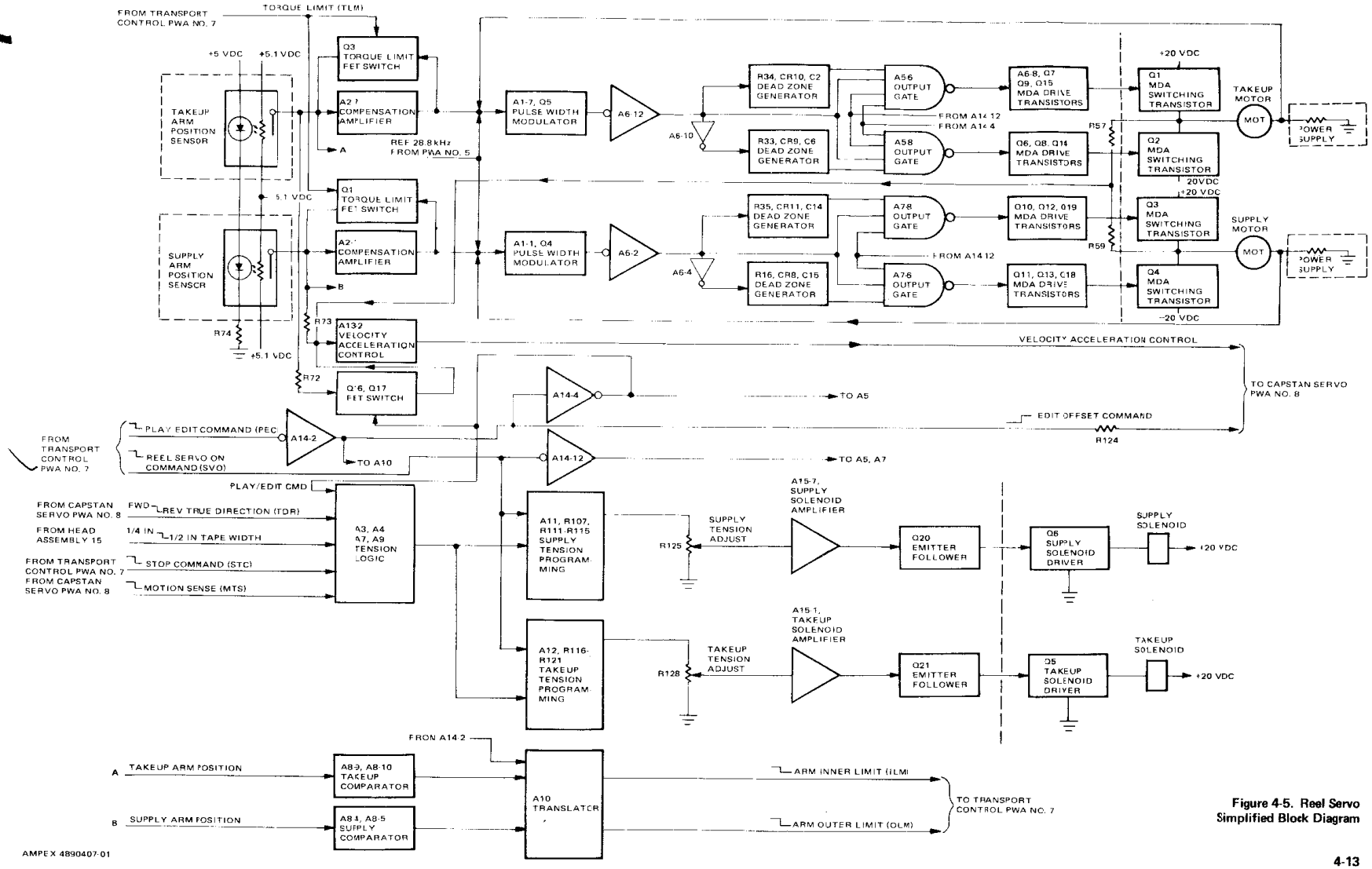


Figure 4-5. Reel Servo Simplified Block Diagram

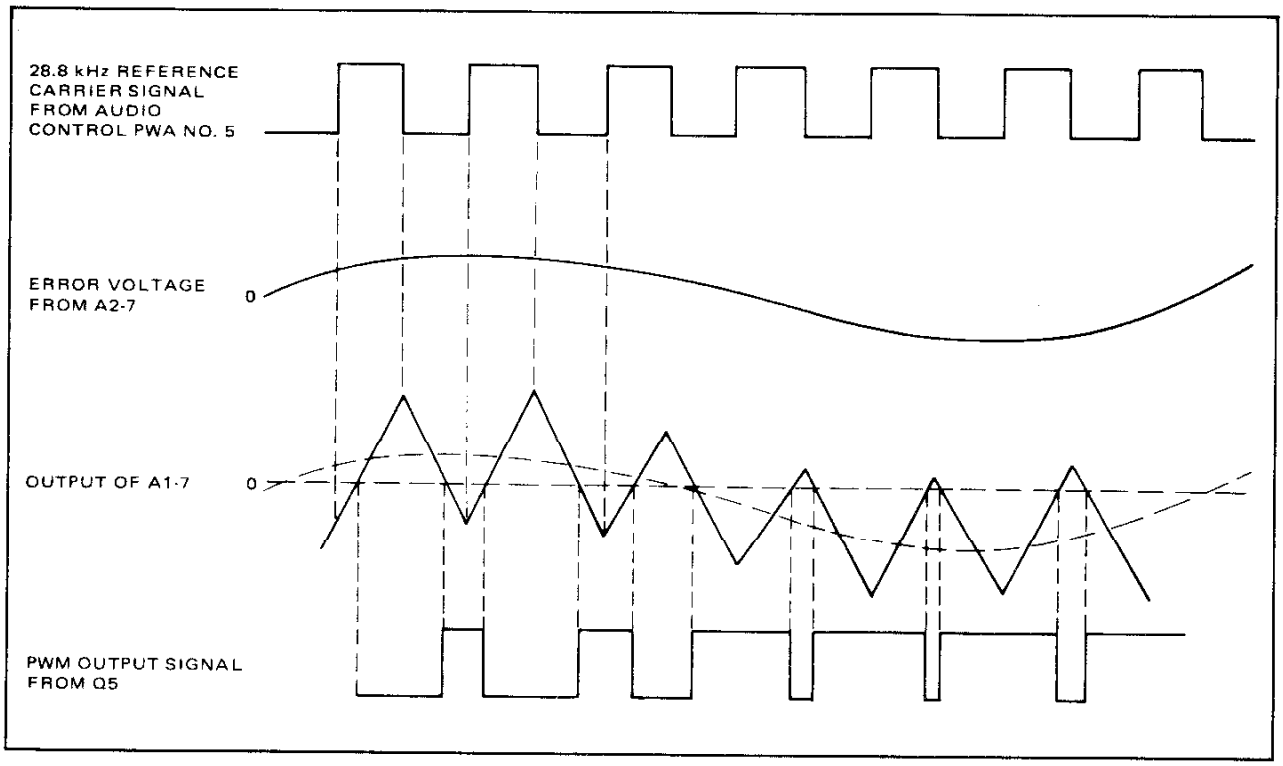


Figure 4-6. Pulse Width Modulator Waveforms, Takeup Reel Servo

supply. The dc component of the sampled signal provides feedback and is applied to the inverting summing input of pulse-width modulator A1-7 to enable the modulator/MDA to be a current source for the motor. For any given error voltage, the feedback provides for constant motor torque at all operating speeds.

4-28. Tension Arm Limit Detector. During recorder operation, if the tension arms should move too far in toward the head assembly (inner limit – ILM) or too far out toward the reels (outer limit - OLM), a logic low ILM or OLM command is generated. These commands are routed to transport control PWA No. 7. The ILM command causes the recorder to immediately enter the stop/edit mode and the OLM command causes the recorder to enter the stop/edit mode after an approximate two-second time delay.

The operation of the takeup and supply tension arm limit detectors are similar in operation, therefore only the takeup detector circuit is described. The voltage sensed by the photopotentiometer is routed to the non-inverting and inverting input of comparators A8-9 and A8-10 respectively. These comparators are referenced to a zener-controlled reference voltage source. When a tension arm limit voltage is exceeded, the associated comparator changes state and applies +12 Vdc to monolithic transistor array A10, which serves as a translator. The translator provides a logic low ILM or OLM command which is routed to transport control PWA No. 7.

During play/edit mode, the takeup tension arm roller is pressed against the capstan. In this mode the takeup arm ILM command is disabled. The logic low play edit command (PEC) is inverted by A14-2 and is applied to transistor A10-4. The transistor turns on and disables the output from comparator A8-9. This causes the ILM command to remain in a high (inactive) state. (The supply tension arm ILM command is still functional.)

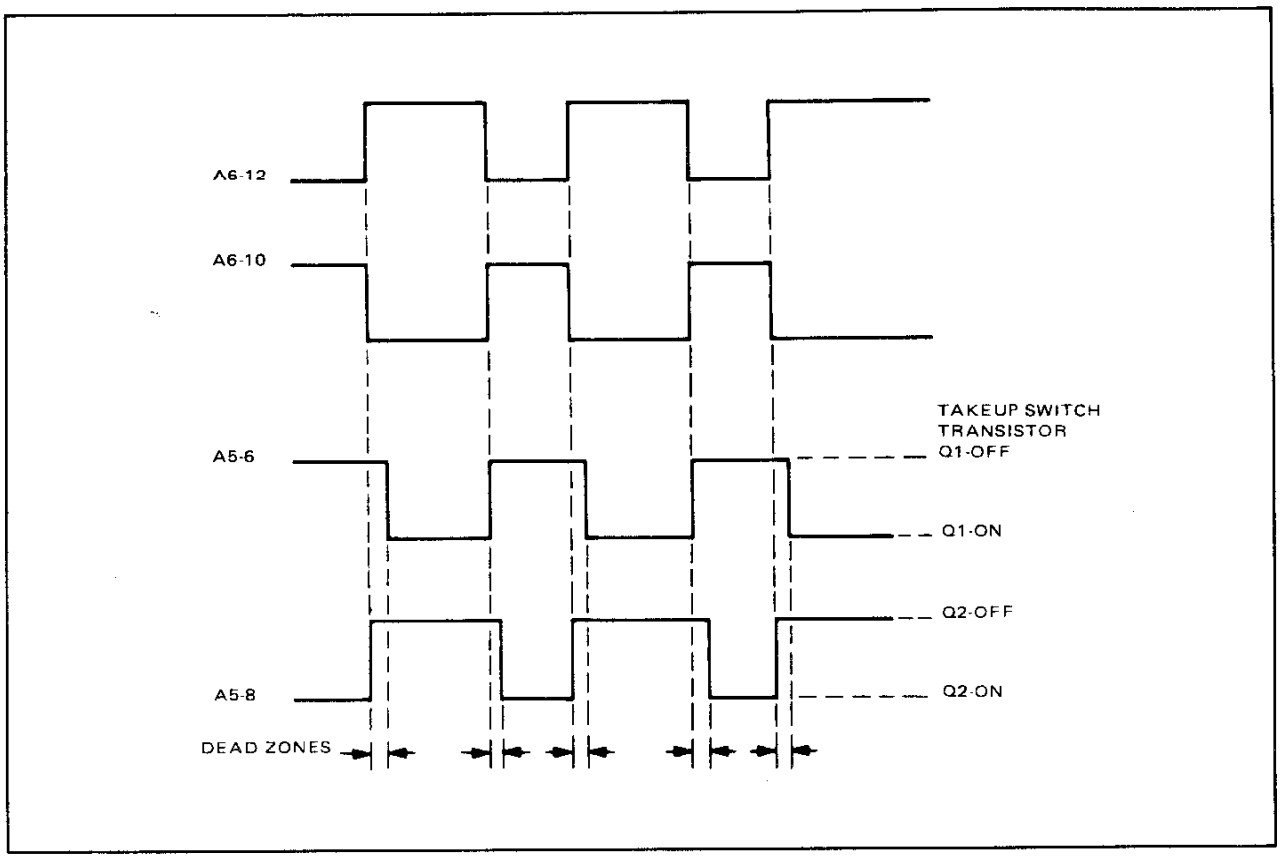


Figure 4-7. Dead Zone Generator Operation and MDA Switch Transistor Conduction State

4-29. Tension Logic. The tension arms exert a constant selected force against the tape, which is balanced through the tape by the torque from the reel motors. This tension has to be the same on the supply and takeup side of the capstan during all modes of operation to prevent tape slippage across the capstan. The tension logic (A3/A4/A7/A9) accepts input signals from six sources and determines what the tape tension should be for a given operating condition. These logic input signals are: motion sense (MTS), stop command (STC), tape width (1/4- or 1/2-inch tape), forward or reverse true direction (TDR), play/edit command (PEC), and reel servo on command (SVO). When 1/2-inch tape is used, the tensions are doubled in forward and reverse modes, but the tension is the same as for 1/4 inch tape when the tape is stopped or when in play/edit mode.

The tension logic performs combinational logic functions and the output is fed to the tension programming. The tension programming consists of six open collector inverters (A11) and associated pull-up resistors (R107 and R112 through R115) for the supply tension; and A12 and R116 through R118, R120, and R121 for the takeup tension. In operation, one of the pull-up resistors is switched into a voltage divider circuit in conjunction with R111 (supply) or R119 (takeup). To select a particular tension, a gate is enabled and the output signal is inverted. The low at the output of the inverter provides a ground return for the selected pull-up resistor. The voltage at the junction of the pull-up resistor and R111 (supply) or R119 (takeup) is applied through a tension adjustment potentiometer R125 (supply) or R128 (takeup) to an operational amplifier A15-7 (supply) or A15-1 (takeup) where the

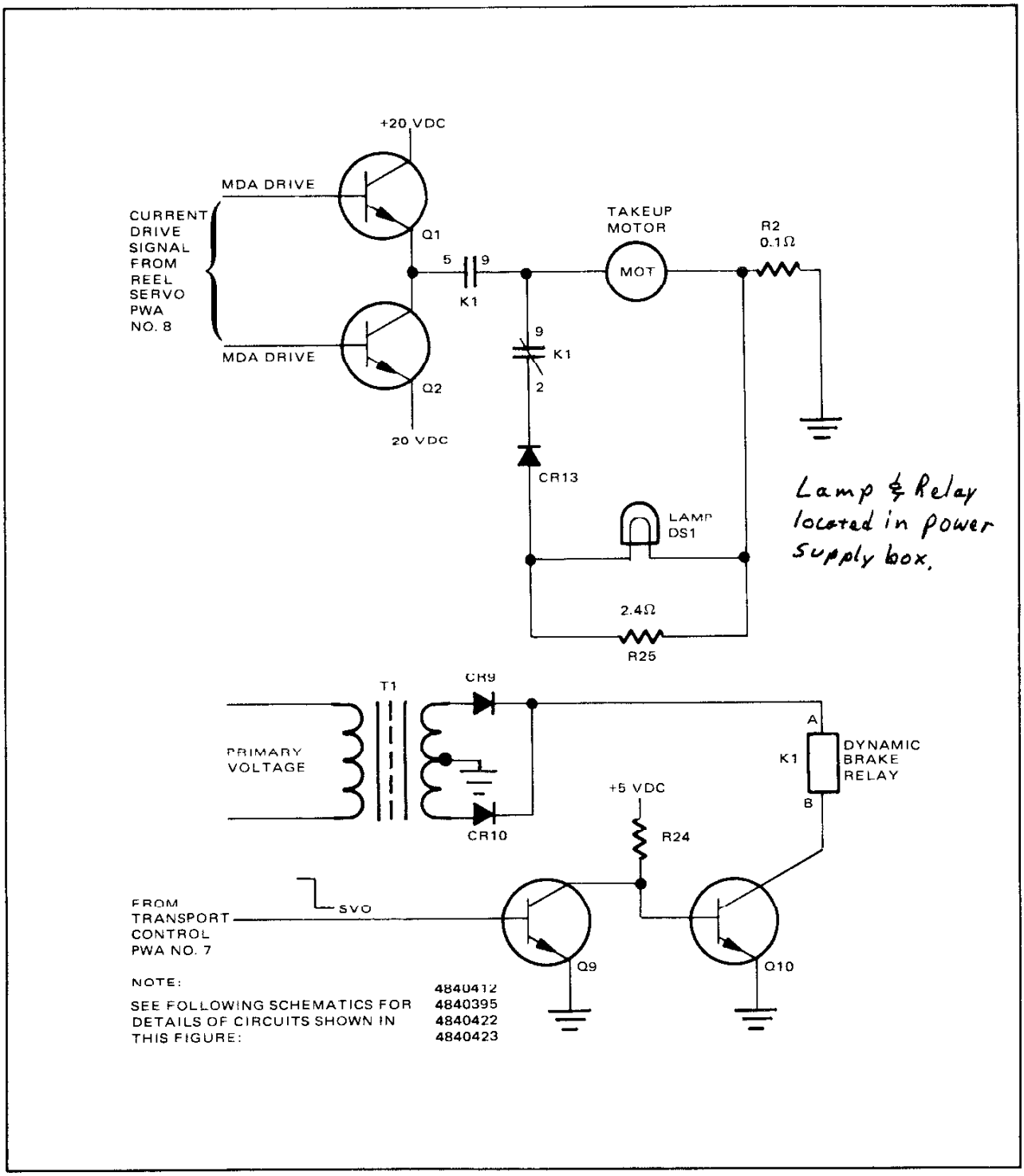


Figure 4-8. Takeup Dynamic Brake, Simplified Schematic

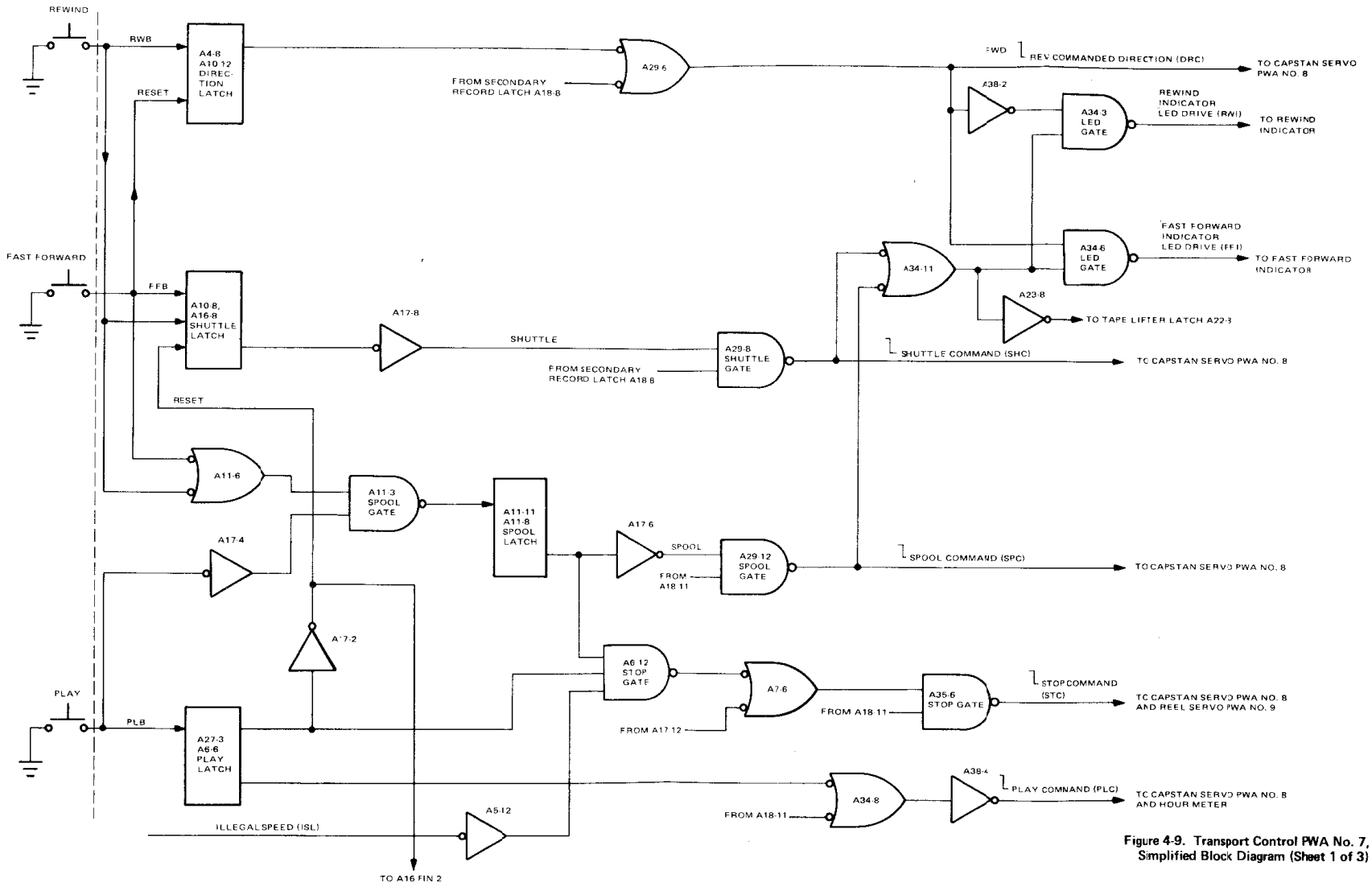


Figure 4-9. Transport Control PWA No. 7, Simplified Block Diagram (Sheet 1 of 3)

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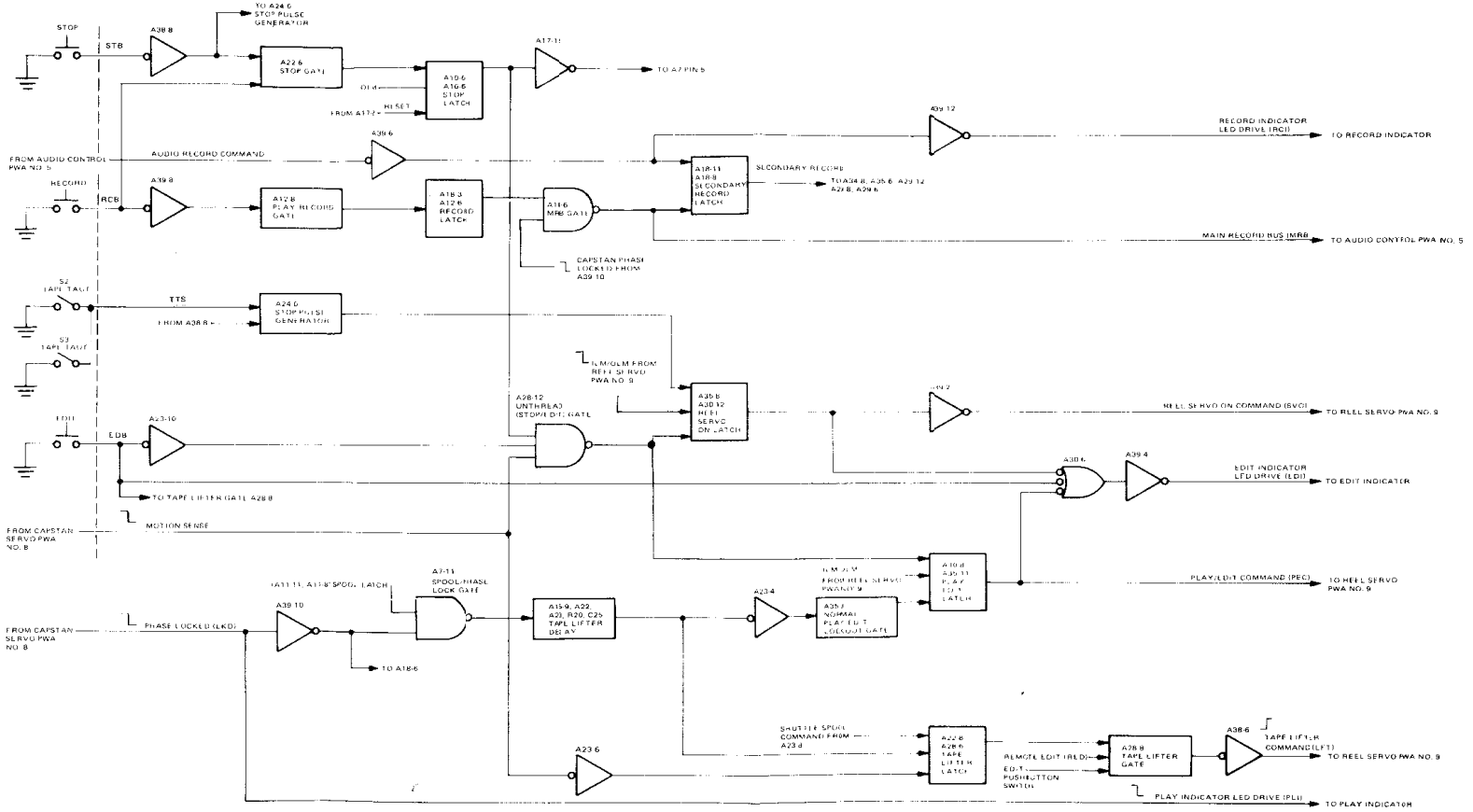

Figure 4-9. Transport Control PWA No. 7, Simplified Block Diagram (Sheet 2 of 3)

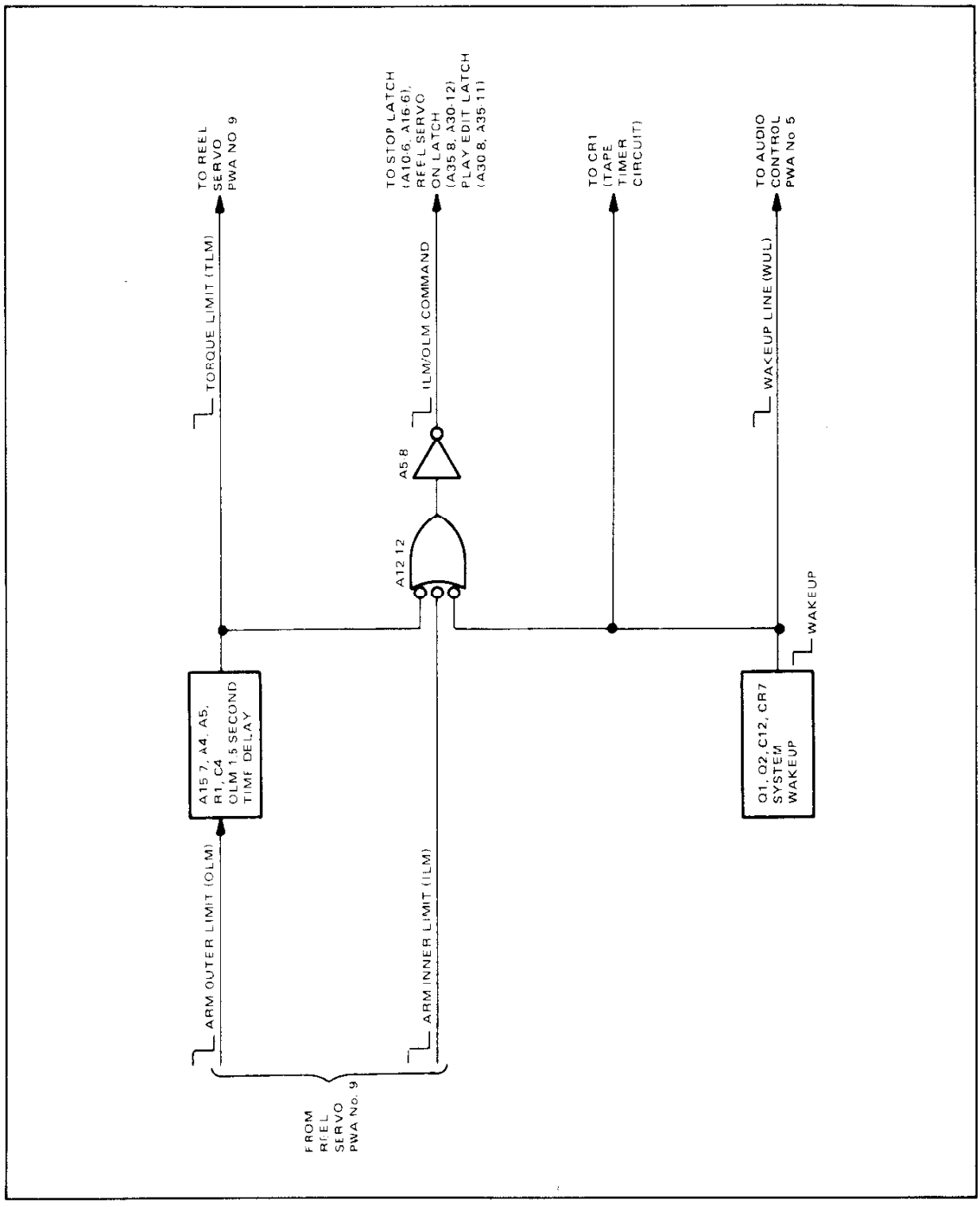

Figure 4-9. Transport Control PWA No. 7, Simplified Block Diagram (Sheet 3 of 3)

In spool modes, the low from A11-8 of the spool latch is inverted by A17-6 and enables spool gate A29-12. The low from A29-12 is inverted by A34-11 and A23-8 to set tape lifter latch A22-8/A28-6 which causes the tape lifter solenoid to be energized (LFT logic high) by the same circuit action as described for shuttle modes.

If shuttle or spool mode is active, pressing the EDIT pushbutton causes the tape lifters to retract (solenoid de-energizes) and the tape to contact the heads as long as the EDIT pushbutton is held pressed. Pressing the EDIT pushbutton switch generates a low which disables gate A28-8. The high from A28-8 is inverted by A38-6 and a low tape lift command (LFT) is routed to reel servo PWA No. 9.

If in fast forward or forward spool mode, and play mode is selected, the tape slows down to play speed (tape does not stop) and the tape lifter solenoid is de-energized (LFT logic low) when the tape reaches play speed. The tape lifter latch A22-8/A28-6 is reset, causing the tape lifter to retract (LFT logic low), by the following circuit action. The high from A11-8 (when not in a spool mode) of spool latch A11-11/A11-8 is applied to pin 13 of A7-11. When coming out of fast forward mode and the tape slows down to play speed, the capstan servo locks and the LKD command from the capstan servo goes low. This signal is inverted by A39-10 and enables gate A7-11. The low from A7-11 is inverted by A23-12 and triggers a 100-ms tape lifter delay circuit consisting of components A15-9/A22-3/A23-2/A22-11/R20/C25. The output of the delay circuit resets the tape lifter latch (pin 4 of A28-6).

To enter play mode from spool mode, the stop pushbutton is pressed followed by the immediate pressing of the play pushbutton. Except for the LKD (servo locked command) the circuit action is the same as described for fast forward to play mode. In spool mode, the capstan servo is phase locked (LKD logic low). When the stop pushbutton is pressed, the capstan servo does not immediately unlock. The 100-ms tape lifter delay circuit has the function of ignoring the LKD command until the servo can unlock when going from spool to stop. Without the time delay, the tape lifter would immediately retract when the stop pushbutton switch was pressed.

If stop mode is selected from any other mode and the tape is permitted to stop, the tape lifter latch is reset by the motion sense command (MTS) which goes high when the tape has stopped. This signal is inverted by A23-6 and resets the tape lifter latch (pin 3 of A28-6).

4-39. Play Mode. Pressing the play pushbutton switch causes play latch A7-3/A6-6 to set, and the low output at A6-6 is inverted by A34-8 and A38-4 to provide a logic low play command (PLC) that is routed to the capstan servo PWA No. 8.

4-40. Record Mode. Record mode is selected by simultaneously pressing the play and record pushbutton switches. Under this condition, gate A12-8 is enabled and sets record latch A18-3/A12-6. The high from A18-3 is applied to gate A18-6 which is enabled by the LKD signal from the capstan servo and signifies the capstan servo is locked.

The low from A18-6 sets secondary record latch A18-11/A18-8 and is also routed as a main record bus (MRB) command to audio control PWA No. 5 to enable the record signal electronics. The low output from A18-11 forces the forward direction (DRC) and play (PLC) commands to be generated. These signals are routed to the capstan servo. When record mode is established, a low electronic record status (ERS) signal from PWA No. 5 is received. This low is inverted by A39-6 and A39-12 and routed to the record indicator (RCI) to illuminate the indicator and signify that record mode has been established. When in record mode and the stop pushbutton switch is pressed, transport motion does not stop until the bias and erase signals applied to the record and erase heads, respectively, have decayed (ERS command goes high).

When the stop pushbutton switch is pressed, stop latch A10-6/A16-6 is set and record latch A18-3/A12-6 is reset. When the record latch resets, gate A18-6 is disabled (MRB goes high), which disables the record signal electronics control on PWA No. 5. A high from stop latch A10-6 is inverted by A17-12 and A7-6 and is applied to stop gate A35-6. After the bias signal has decayed, the ERS signal from PWA No. 5 goes high and resets the secondary record latch, and a high from A18-11 enables stop gate A35-6. When A35-6 is enabled,

a logic low stop command (STC) is generated and routed to the capstan servo and reel servo PWAs to stop tape motion.

4-41. Stop Record Mode. If in record mode and the record pushbutton switch is held pressed while the stop pushbutton switch is momentarily pressed, the recorder will stop recording but the transport will continue to run. Tape motion stop is prevented by inhibiting gate A22-6 with a logic low that is generated when the record pushbutton switch is pressed. The record latch is reset via gates A6-8 and A17-10 when the stop pushbutton switch is pressed.

4-42. Thread Mode. When power is initially applied and tape is threaded and taut so that either parallel connected microswitches S2 (supply) or S3 (takeup) are closed, pushing the stop pushbutton switch causes the reel servos to activate and place transport in a thread mode condition. Thread condition is indicated by the EDIT indicator light going off when the stop pushbutton is pressed.

Pressing the stop pushbutton switch causes one shot A24-6 to generate a 0.5-second logic low pulse which sets reel servo on latch A35-8/A30-12. The one-shot is used to assure ample time for the tension arms to move off the outer limit. The high from A35-8 is inverted by A39-2 to generate a logic low reel servo-on command (SVO), which is routed to reel servo PWA No. 9 to activate the reel servos. When the reel servo-on latch is set, the high from A35-8 is inverted by A30-6 and A39-4 and the EDIT indicator light goes out.

4-43. Unthread (Stop/Edit) Mode. If the tape is stopped, pressing the EDIT pushbutton switch causes the recorder to go into the unthread (same as stop/edit) mode. In this mode, the reel servos disengage. Pressing the EDIT pushbutton switch generates a logic low which is inverted by A23-10 which causes A28-12 to be enabled. The low from A28-12 resets reel servo latch A35-8/A30-12, which causes the reel servo on command (SVO) to be cancelled (SVO logic high). The low from A35-8 is inverted by A30-6 and A39-4 (EDI) to activate the EDIT indicator.

4-44. Edit Modes. If in play or record mode (capstan is phase locked) and the EDIT pushbutton switch is pressed, power will be removed from the takeup reel and the tension-arm roller will engage the capstan. This is called the play/edit mode.

Pressing the EDIT pushbutton switch generates a logic low, which is inverted by A23-10 and routed through a jumper in the E12/E13 position to enable gate A35-3 when the capstan servo is locked. The output from A35-3 sets play/edit latch A35-11/A30-8, and a low PEC (play/edit) command from A30-8 is routed to the reel servo. The low from A30-8 is inverted by A30-6 and A39-4 (EDI) to activate the EDIT indicator.

If in play/edit mode and the stop pushbutton is pressed, the tape will stop, edit mode will be retained, and tape can again be spilled by pressing the play pushbutton switch.

To cancel play/edit mode, the EDIT pushbutton switch is pressed when the tape is stopped. When the tape is stopped, the motion sense (MTS) line is high and the stop latch is set. Therefore, pressing the EDIT pushbutton switch enables A28-12. The low from A28-12 resets the play/edit latch and the servo-on latch which causes the recorder to enter the stop/edit (or unthread) mode. If desired to lockout the play/edit mode, the jumper may be placed in the E13/E14 play edit lockout position. This disables gate A35-3 and prevents the play/edit latch from being set.

If shuttle or spool mode is active, pressing the EDIT pushbutton switch causes the tape lifters to retract (solenoid de-energizes) and tape contacts the heads as long as the EDIT pushbutton switch is held pressed (see *Tape Lifter Operation* text).

When using the remove control unit to control recorder functions, the only edit function permitted is control of the tape lifters in shuttle or spool modes. The play/edit and stop/edit modes may not be activated from the remote control unit. On the remote control unit, the EDIT pushbutton switch is connected to transport control PWA No. 7 via the remote edit line (RED) rather than the edit button line (EDB).

4-45. Tension Arm Limit Detectors. During recorder operation, if a condition exists where the tension arms should move in too far towards the

head assembly or too far out toward the reels, a logic low ILM (inner limit) or OLM (outer limit) command is generated on the reel servo PWA No. 9 and routed to the transport control PWA No. 7. The ILM command causes the recorder to immediately enter the stop/edit (unthread) mode and the OLM command causes the recorder to enter the stop/edit mode after an approximate 1.5-second time delay.

The ILM command is inverted by A12-12 and A5-8 and sets the stop latch and resets the reel servo on latch and the play/edit latch. The OLM command is applied to a time delay circuit consisting of 1.5-second one-shot A15-7 and components A4-3/A5-4/A4-6/R1/C4. If the OLM command is low for more than 1.5 seconds, the recorder will enter the stop/edit mode as described for the ILM command.

During the start of thread mode, the OLM command is low and the delayed OLM command from A4-6 is routed as a torque limit command (TLM) to reel servo PWA No. 9 to limit the unwinding reel torque during the start of thread mode.

4-46. Audio Control PWA No. 5

The audio control PWA No. 5 performs the following functions:

1. Accepts mode and channel selection commands from the control unit and performs combinational logic functions to establish desired mode of operation.

2. Generates a master frequency of 5.1840 MHz which is divided down and used to provide reference frequencies for the capstan and reel servos, bias and erase amplifiers, and clock frequencies for the tape timer and multiplexer.

3. Conditions master bias bus signals and erase bus signals for distribution to the audio PWAs.

The functions performed by PWA No. 5 are shown on simplified block diagrams. For complete circuit information, refer to PWA No. 5 schematic diagram 4840398.

4-47. Signal Mode Selection. Figure 4-10 is a simplified interconnection block diagram of the signal mode selection circuits and Figure 4-11 is a simplified block diagram of the signal mode selection circuits for channel 1. Figure 4-11 shows the relationship and functions of the various circuits that operate to establish a recorder/reproducer signal mode of operation and associated signal mode monitoring. The desired signal mode and channel(s) are selected by pressing pushbutton switches on the recorder control unit. These command signals are routed to audio control PWA No. 5 to program the desired mode of operation. PWA No. 5 contains four separate mode select circuits, one for each channel. Since each circuit operates identically, only channel 1 is described in detail.

There are four channel-select lines (channels 1-4) and five function-select lines (ready, safe, sync, repro, and input). Pressing the associated pushbutton switch generates a logic low command which is routed to PWA No. 5. These momentary command signals are stored in latch circuits and processed by combinational logic to provide four two-state logic commands which are routed to main audio PWA No. 1 (for channel 1). Output signals for some of the various functions are summarized in Table 4-5.

4-48. Latches. The momentary commands, generated when a channel select and a function select pushbutton switch are simultaneously pressed, cause the command to be stored in a latch. Each of these latch circuits have one output, but some have more than one set or reset input to provide various modes of operation as determined by the combinational state of the latches. The following latches are associated with channel 1 operation.

4-49. Ready/Safe Latch. The ready/safe latch A9-7 is set by a ready command and reset by a safe command.

4-50. Sync/Rep Latch. The sync reproduce latch A9-13 is set by a sync command and reset by a reproduce command.

4-51. Tape/Input Latch. The tape/input latch A9-4 is set by either a reproduce or sync command and is reset by an input command.

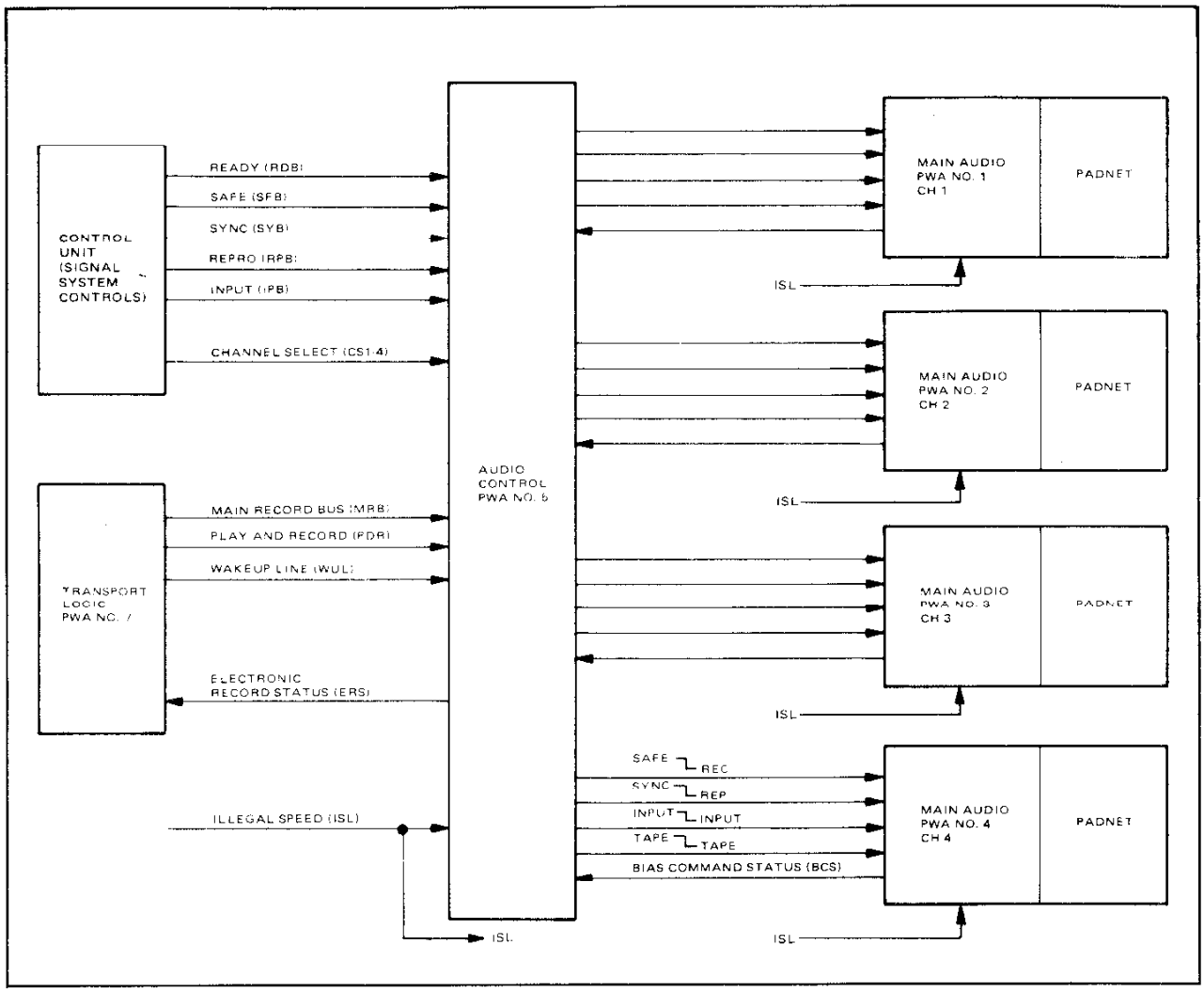

Figure 4-10. Signal Mode Selection, Interconnection Simplified Block Diagram

4-52. Safe/Record Latch. The safe/record latch A9-9 is set (to safe) by any one of the following commands: main record bus (MRB), wakup line (WUL), safe command, or ready command. The latch is reset when the following three conditions are present: ready/safe latch is in the ready (set) state, main record bus (MRB) is active, and play and record (PDR) command is active.

4-53. Safe Mode. In safe mode, the channel is prevented from entering record mode. Simultaneously pressing SAFE and channel 1 pushbutton switches enables gate A10-8. The low from A10-8 resets ready/safe latch A9-7 to the safe state. The low from A10-8 is also inverted by A8-6 and A6-8 and sets safe/record latch A9-9 to the safe state. The high from A9-9 is buffered by A5-8 and routed to PWA No. 1 to place the audio electronics in a safe (record mode inhibited) condition. The low from A9-7 inhibits record interlock gate A8-8. This prevents the safe/record latch A9-9 from being reset to the record state if the play and record pushbuttons are simultaneously pressed to place other channels in the

record mode. The low from A9-7 is also routed to the multiplexer (paragraph 4-61) to cause the SAFE indicator to illuminate.

4-54. Ready Mode. A channel in ready mode can enter record mode. Simultaneously pressing READY and channel 1 pushbutton switches enables gate A10-6. The low from A10-6 causes ready/safe latch A9-7 to set, and the high from A9-7 is applied as one input to three-input record-interlock gate A8-8 to establish conditions for entering record mode (described later). The low from A10-6 is also applied to the multiplexer to cause the channel 1 READY indicator to illuminate. The low from A10-6 is also inverted by A8-6 and A6-8 to set safe/record latch A9-9 to the safe position for the same purpose as described for safe mode. That is, it enables the safe/record latch A9-9 to be temporarily placed in the safe mode with ready/safe latch A9-7 left in ready mode.

4-55. Record Mode. To enter record mode, the channel must be in ready mode and the PDR (play and record) and MRB (main record bus) lines active (logic low). When the play and record pushbuttons are simultaneously pressed, the PDR line becomes active and triggers 900-ms one-shot A32-6. The high from A32-6 is applied as a second input to A8-8. Approximately 150 to 500 ms (up to 500 ms if tape is stationary) after the two pushbuttons are pressed, the MRB line becomes active, indicating the capstan servo has locked. The MRB logic low is inverted by A40-6, A8-8, and resets safe/record latch A9-9 to the record position. The low from A9-9 is buffered by A5-9 and routed to main audio PWA No. 1 to place the audio electronics in the record mode. Immediately prior to the bias signal runup to maximum level, a low BCS (bias command status) command from PWA No. 1 enters PWA No. 5 and is inverted by A6-2, A6-4, A34-6 and A27-6 and routed to transport control PWA No. 5 as a low ERS (electronic record status) command signal. This signal causes the master record indicator to illuminate. Also the low BCS command at the junction of A6-4 and pin 5 of A34-6 is routed to the multiplexer to cause the channel 1 record indicator to illuminate. The illumination of the master record and the channel 1 record indicators is a positive indication that the record process has occurred on PWA No. 1.

If an MRB signal is not received within the 900-ms window established by one-shot A32-6, gate A8-8 is inhibited and the system does not enter record mode. One-shot A32-8 is reset when the MRB signal arrives. The output from the one-shot and the inverted MRB signal are applied to gate A40-3. The gate is enabled by the MRB signal and the output from A40-3 resets one-shot A32-6. The width of the pulse applied to pin 10 of safe/record latch A9-9 is approximately 300 ns long and is equal to the propagation delay through A40-3 and A32-6 plus the time delay caused by R35 and C18, which are used to widen the width of the pulse applied to the clear input of A32-6.

When in record mode and the stop pushbutton is pressed, the transport does not stop until the bias and erase signals have decayed. When the stop pushbutton switch is pressed, MRB goes high and causes the safe/record latch A9-9 to be set to the safe position. The high from A9-9 is buffered by A5-8 and routed to PWA No. 5 to place the signal electronics in the safe mode. After the bias and erase signals have decayed, the BCS command goes high causing the ERS command to go high. The high ERS command is routed to transport control PWA No. 7 to reset the secondary record latch which causes the transport to come to a stop.

If in record mode and the ready and channel 1 pushbutton switches are simultaneously pressed, the channel 1 signal electronics will revert to safe but the transport will continue to run. Pressing the two pushbuttons causes safe/record latch A9-9 to be set to the safe position. The high from A9-9 is buffered by A5-8 and routed to PWA No. 5 to place channel 1 signal electronics in the safe mode. Since the ready/safe latch A9-7 is still in the ready state, channel 1 may be returned to record mode by simultaneously pressing the play and record pushbutton switches. When these pushbuttons are pressed, the safe/record latch A9-9 is reset to the record state.

If in record mode and the safe and channel 1 pushbutton switches are simultaneously pressed, channel 1 signal electronics will revert to safe but the transport will continue to run. Pressing the two pushbuttons causes the ready/safe latch A9-7 to be reset to safe and the safe/record latch A9-9 to be set to safe. To re-enter record mode, channel 1 must be reset to the ready state.

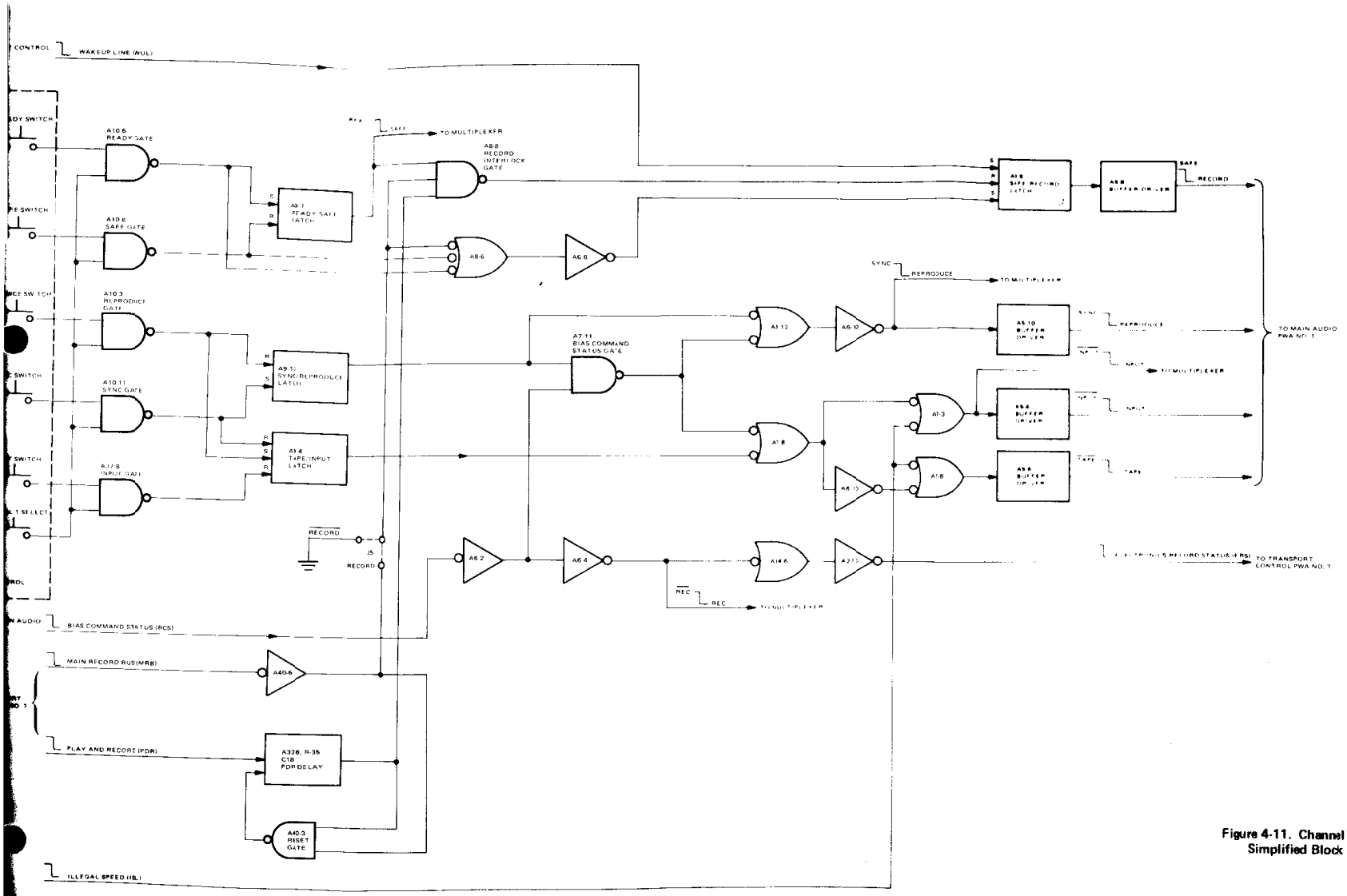

Figure 4-11. Channel 1 Signal-Mode Selection Simplified Block Diagram, Audio Control PWA No. 5

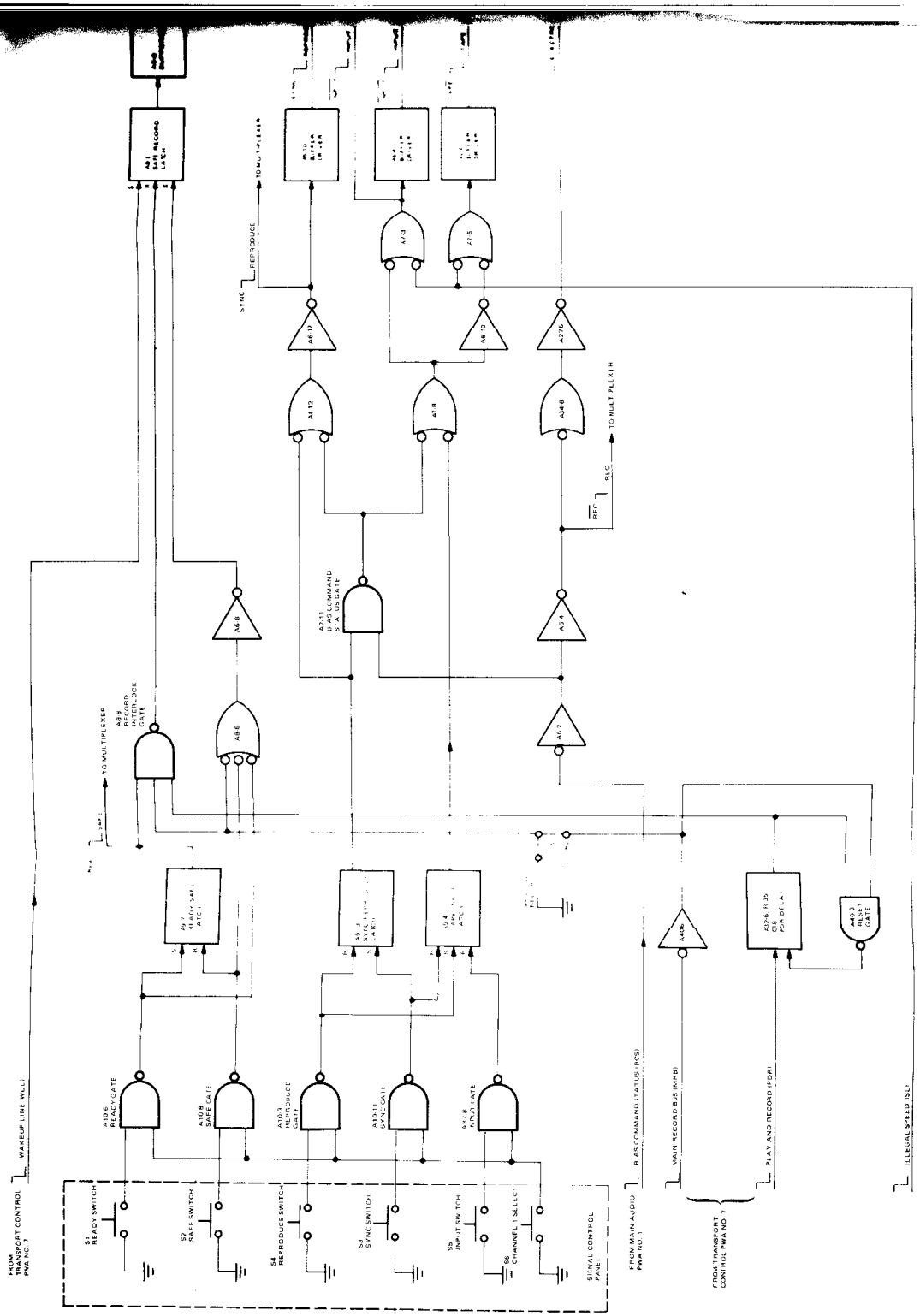

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Table 4-5. Channel 1 Signal Mode Selection Output-Signal Logic States

FUNCTIONS	OUTPUT SIGNAL LOGIC STATE			
	SAFE⌐RECORD (PIN 24)	SYNC⌐REP (PIN 23)	$\overline{\text{INPUT}}$⌐INPUT (PIN R)	$\overline{\text{TAPE}}$⌐TAPE (PIN 14)
INPUT	X	X	L	H
REPRODUCE	H	L	H	L
SAFE	H	X	X	X
READY	H	X	X	X
RECORD	L	L	X	X
SYNC AND READY OR SAFE	H	H	H	L
RECORD FROM SYNC MODE	L	L	L	H

L = low
H = high
X = low or high depending on combination of modes selected

4-56. Reproduce Mode. In reproduce mode, the signal being reproduced by the reproduce head is connected to the audio output. Simultaneously pressing REPRO and channel 1 pushbutton switches enables gate A10-3 which resets sync/reproduce latch A9-13 to the reproduce state. The low from A9-13 is inverted by A8 12 and A6-12, buffered by A5-10 and routed to PWA No. 1 as a low reproduce (rep) command. Also the low at the output of A6-12 is routed to the multiplexer to cause the REPRO indicator to light.

Pressing the two pushbutton switches also causes the tape/input latch A9-4 to set to the tape state. Under this condition, the $\overline{\text{input}}$/input line is high ($\overline{\text{input}}$), and the $\overline{\text{tape}}$/tape is low (tape). Both of these commands are routed to PWA No. 1 to cause the tape signal to be monitored.

4-57. Sync Mode. In sync mode, the signal on tape is reproduced by the record head. Simultaneously pressing SYNC and channel 1 pushbutton switches enables gate A10-11 which sets sync/reproduce latch A9-13 to the sync state. This permits A8-12 to be low and this signal is inverted by A6-12, buffered by A5-10, and routed to PWA No. 1 as a high sync command. The high from A6-12 is routed to the multiplexer to cause the SYNC indicator to light.

Pressing the two pushbutton switches also causes the tape/input latch A9-4 to set to the tape state. As in reproduce mode, the $\overline{\text{input}}$/input line is high ($\overline{\text{input}}$), and the $\overline{\text{tape}}$/tape line is low (tape).

If a channel is in sync mode and that same channel is placed into record mode (channel is in ready and the play and record pushbuttons are simultaneously pressed), the logic circuitry on PWA No. 5 will automatically switch the monitoring circuitry on PWA No. 1 from the record head to the input signal. Pressing the play and record pushbutton switches causes the BCS signal entering PWA No. 5 to become active (low). (See *Record Mode* description.) This signal is inverted by A6-2 and enables A7-11. The low from A7-11 is inverted by A8-12 and A6-12, buffered by A5-10, and routed to PWA No. 1 as a low (rep) command. This disconnects the sync preamplifier from the equalizer amplifier and connects the reproduce head to the equalizer amplifier. The low from A7-11 causes the $\overline{\text{input}}$/input line to be low (input) and the $\overline{\text{tape}}$/tape line to be high ($\overline{\text{tape}}$). This enables the input to be monitored. The low from A7-3 is routed to the multiplexer to cause the INPUT indicator to light.

4-58. Input Mode. When input monitoring mode is selected, the input signal to the recorder is connected to the audio output for monitoring

purposes. Simultaneously pressing the INPUT and channel 1 pushbutton switches enables gate A37-8, which resets tape/input latch A9-4 to the input state. The low at A7-3 is routed to the multiplexer to cause the INPUT indicator to light.

4-59. Wakeup Line. When power is first applied to the recorder, the system wakeup circuit (located on transport logic PWA No. 7) causes the recorder to enter stop/edit mode; tape timer to indicate 0 00 00; SAFE, REPRO, stop, and EDIT indicators to light; and audio channels to enter safe and reproduce modes. When power is first applied, the wakeup line (WUL) becomes active (low) for five seconds. This low is applied to gate A40-11 to inhibit the master bias bus (paragraph 4-64), and the low is also applied through buffer A38 to each of the four channel-select lines and to the safe and reproduce function-select lines. This causes the sync/reproduce latch A9-13 to be in the reproduce state (A9-13 low) and the safe/record latch A9-9 to be in the safe state (A9-9 high). In the event that PWA No. 7 is not installed and power is applied, capacitor C11 will charge through R21 and temporarily apply a low through CR6 to A38 to substitute for the WUL logic low command.

4-60. Illegal Speed. If a speed is selected for which the audio channels have not been set up for (and/or speed and bias jumper positions on audio control PWA No. 5 are incorrect), play and record modes of operation at that speed are locked out of operation. If an illegal speed is selected, the illegal speed line (ISL) becomes active (low). This low is inverted by A7-3 and A7-6 to cause the input/input and the tape/tape lines to both go high. This causes the audio output from all audio PWAs (PWA No. 1, 2, 3, and 4) to be muted.

4-61. Multiplexer System. The multiplexer system accepts mode and channel status information and causes the appropriate LED indicators to be illuminated on the control unit. Figure 4-12 is a simplified interconnection block diagram of the multiplexer system circuitry.

The multiplexer system accepts channel and mode select data from the signal mode selection logic circuitry (paragraph 4-47) and sequentially loads this data in parallel form in two shift registers located on PWA No. 5. This data is shifted out in serial form on a single line to six series-connected shift registers located on the local control unit (and remote control unit if used). The shifted data is used to illuminate the appropriate LED indicator (SYNC, REPRO, INPUT, SAFE, READY and Record). A slow clock rate (4.8 kHz) and a fast clock rate (144 kHz) are alternately used in the multiplexer system circuitry to enable the LED indicators to be illuminated continuously 97% of the time.

Figure 4-13 is a simplified block diagram of the multiplexer system circuitry on PWA No. 5. Recall that each of the four channel and mode selection logic circuits provide four two-state logic commands. These commands are $\overline{\text{rec}}$/rec, ready/safe, tape/input and sync/rep. Since there are four audio channels, 16 lines of data (4 X 4) are supplied to the input of two multiplexer devices (A35 and A36). Each multiplexer (A35 and A36) is a dual 4-line-to-1-line data selector and in operation, the combination is synonymous to a 4-pole 4-way switch.

These four logic-state inputs to the multiplexers from each channel are selected in sequence (channel 1, channel 2, etc.). This input signal selection is controlled by a 2-bit binary coded signal (binary 0-3 count) applied to the select A and select B inputs of the multiplexer devices. (The source of this binary signal is described later.) The strobe (enable) input to each multiplexer is hard wired low and therefore the multiplexers are continuously enabled.

The four selected signals from the output of the two multiplexers are applied to four NAND gates (A42-3, -6, -8, and -11) that perform combinational logic to provide six signals. These six signals are applied to the parallel inputs of shift registers A33 and A41, and each signal corresponds to an LED indicator on the control unit (SYNC, REPRO, INPUT, SAFE, READY, and Record). A low state of the input signal signifies that the associated LED indicator is to be illuminated.

In addition to the six data line inputs from the combinational logic, there are three hard-wired inputs applied to shift register A33. Input A and the serial input are hard-wired high (+5 Vdc) and input B is hard-wired low (ground). These inputs

are used to identify when a frame of data has been shifted through the shift registers.

When the mode control input signal (described later) applied to the shift registers goes high, the input data and the high on input A and the low on input B are loaded into the shift registers on the next high-to-low transition of the input clock pulse. During this parallel load sequence, the entry of serial data is inhibited (this is accomplished internally in the shift registers by the high mode-control signal). The loading of data causes the mode control to go low, which permits the data to be shifted serially. The next six clock pulses cause the channel data to be serially shifted through the shift registers and sent in serial form (from pin 10 of A41) to the first six cells of six series-connected serially-loaded shift registers located on the control unit.

As the data is shifted (direction A toward D), the hard-wired high applied to the serial input of A33 is also shifted until there are four adjacent high outputs from the shift register preceded by the hard-wired low. After a frame of data six bits long has been shifted through the shift register, the four adjacent highs enable gate A34-8 which serves as a channel frame detector. (Note that the data input can never be four adjacent highs.)

When A34-8 is enabled, the low from A34-8 is inverted by A2-8 and is applied as a high to the mode control input of the shift registers. This changes the shift register mode of operation from serial shift to parallel load and enables the shift registers to load the next set of data (channel 1) from the multiplexers when the binary-coded select A and select B lines change state.

At the end of a frame of data, the low from A34-8 is also used to clock a binary counter, formed by A4-12 and A25-8, to its next state to enable the multiplexers to select data from the next channel (channel 2). The output from divider A4-12 and A25-8 is supplied to the select A and B inputs of the multiplexers.

In addition, the low from A34-8 is applied to gate A26-11 which inhibits the fast rate clock from divider A4-8 (through gate A26-6) during parallel load time. When A34-8 is high, the fast rate clock is routed to the control unit to clock the six series-connected shift registers. (Note: Only the fast rate clock is routed to the control unit.) After the data from all four channels has been shifted into the six shift registers on the control unit, the multiplexers and shift registers on PWA No. 5 repeat the four-channel sequence but are controlled by the slow rate clock. Also during this slow rate clock sequence, the gated clock signal normally supplied to the six series-connected shift registers on the control unit is held high (inhibited by a low from A25 pin 6) to prevent the data from being entered during the slow clock sequence. As the ratio of the clock signals (4.8 kHz and 144 kHz) is 30:1, the LED indicators are continuously illuminated 97% (duty cycle) of the time.

As previously stated, the 144-kHz clock and 4.8-kHz clock are alternately used after each four-channel sequence. The output from frame detector A34-8 is divided by A4-12 and A25-8 and fed to D flip-flop A25-5 which provides complementary outputs. These outputs are used to alternately enable gates A26-3 and A26-6, which enable the 4.8 kHz clock and the 144 kHz clock, respectively. The selected clock is inverted by A26-8 and applied to one-shot A32-10 which provides a clean fixed-width pulse used to clock shift registers A33 and A41. The clock-pulse edge used to clock A33 and A41 occurs earlier than the clock edge used to clock the shift registers in the control unit. This permits the data input to the control unit to settle before being strobed.

4-62. Master Oscillator and Counters. The master oscillator generates a frequency of 5.184 MHz which is divided down and used for the following functions: reference frequencies for the capstan servo, switching carrier for the reel servo, audio bias and erase frequencies, and clock frequencies for the multiplexer system circuitry and the tape timer. Figure 4-14 is a simplified block diagram of the master oscillator and counters.

The master oscillator consists of a non-inverting amplifier with positive feedback provided by a crystal resonating at the desired frequency. The non-inverting amplifier consists of inverters A2-2 and A2-4 connected in cascade. Inverter A2-2 serves as a quasi-linear amplifier with inversion between its input and output terminals.

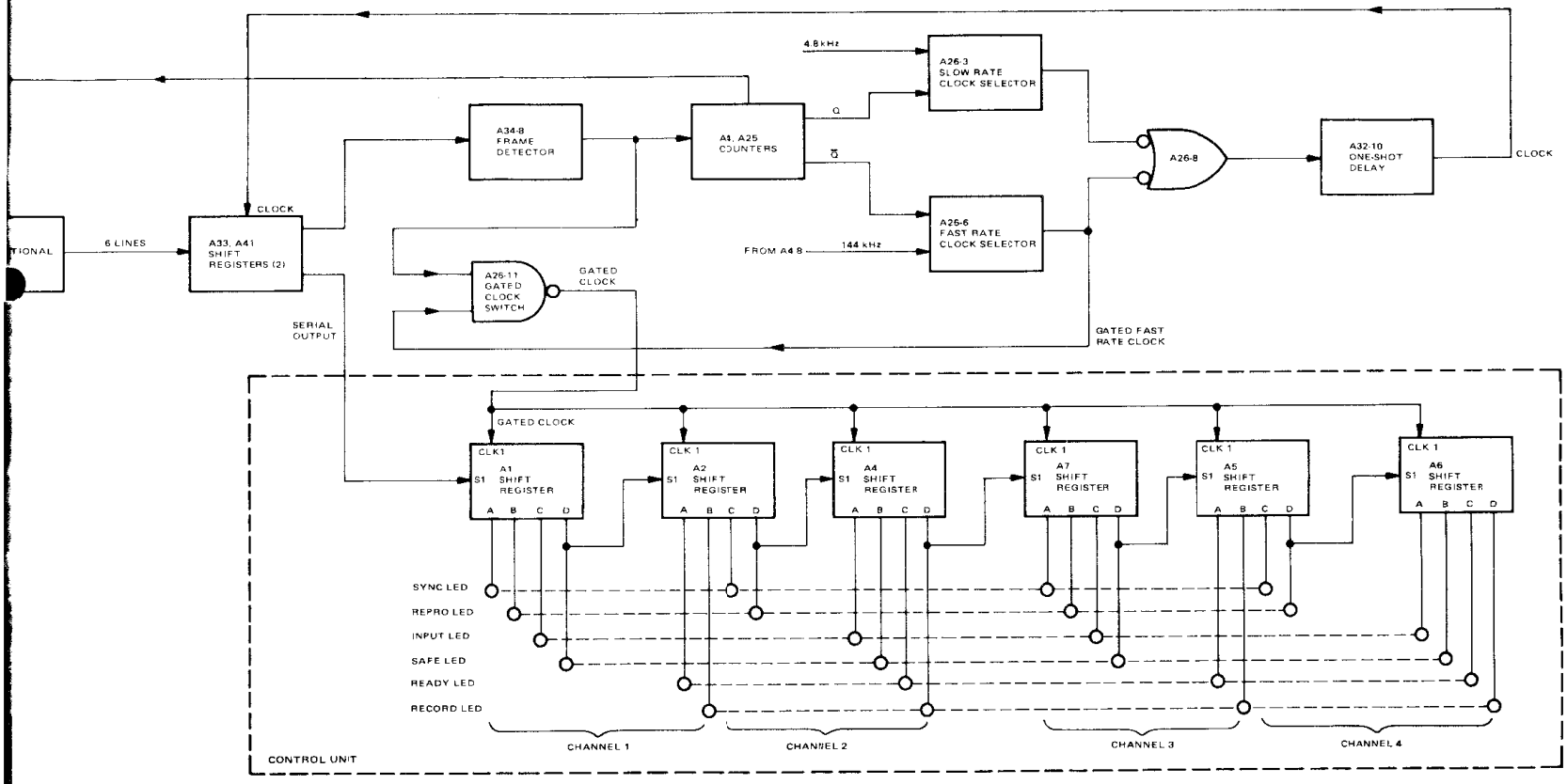
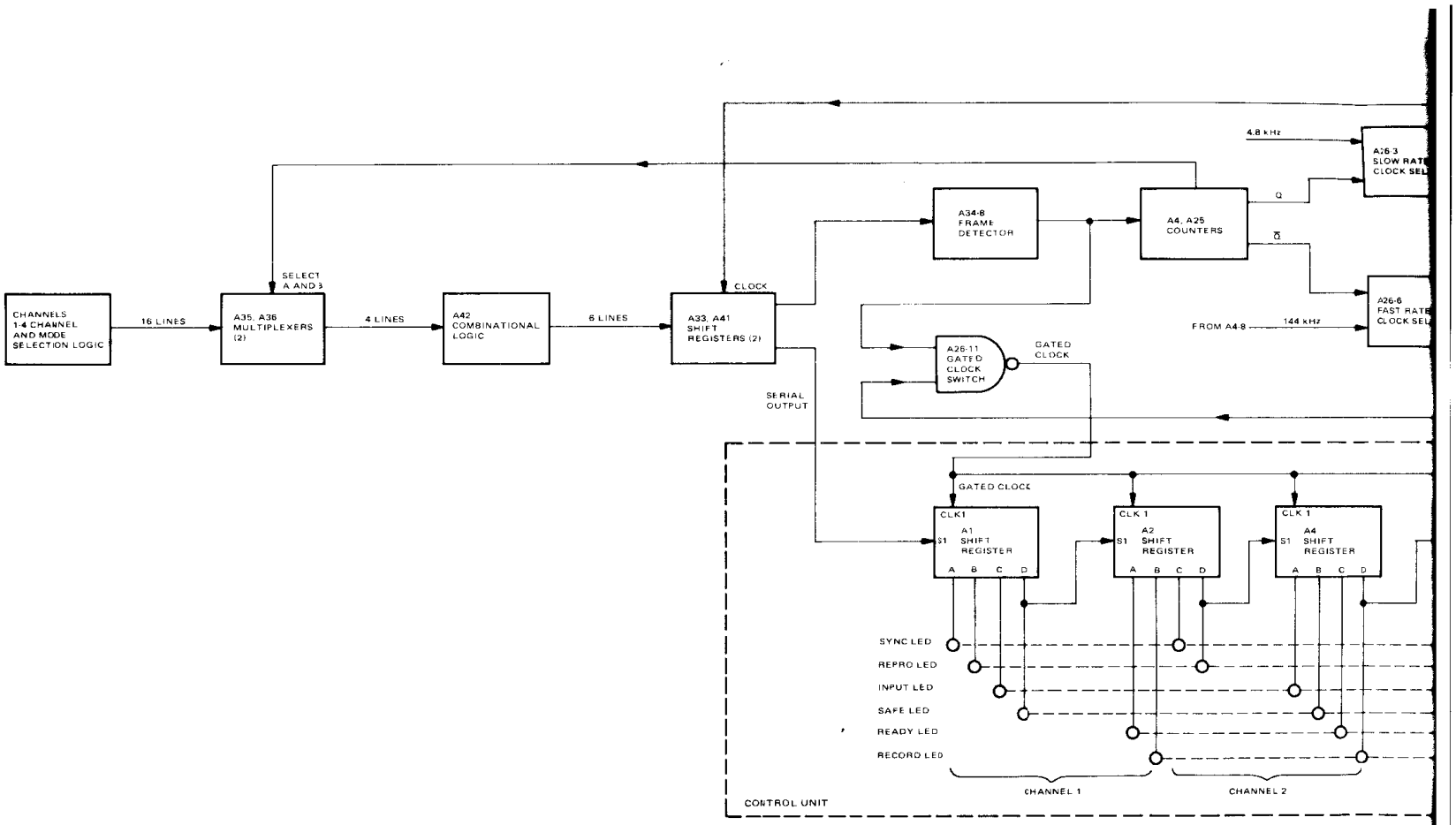


Figure 4-12. Multiplexer Simplified Interconnect Block Diagram, Audio Control PWA No. 5 and Control Unit


CHANNELS 1-4 CHANNEL AND MODE SELECTION LOGIC
16 LINES
A35, A36 MULTIPLEXERS (2)
SELECT A AND B
4 LINES
A42 COMBINATIONAL LOGIC
6 LINES
A33, A41 SHIFT REGISTERS (2)
CLOCK
SERIAL OUTPUT
A34-8 FRAME DETECTOR
A4, A25 COUNTERS
Q
Q̄
4.8 kHz
A26-3 SLOW RATE CLOCK SEL
A26-6 FAST RATE CLOCK SEL
FROM A4-8
144 kHz
A26-11 GATED CLOCK SWITCH
GATED CLOCK
GATED CLOCK
CLK1
S1
A1 SHIFT REGISTER
A2 SHIFT REGISTER
A4 SHIFT REGISTER
A B C D
SYNC LED
REPRO LED
INPUT LED
SAFE LED
READY LED
RECORD LED
CHANNEL 1
CHANNEL 2
CONTROL UNIT

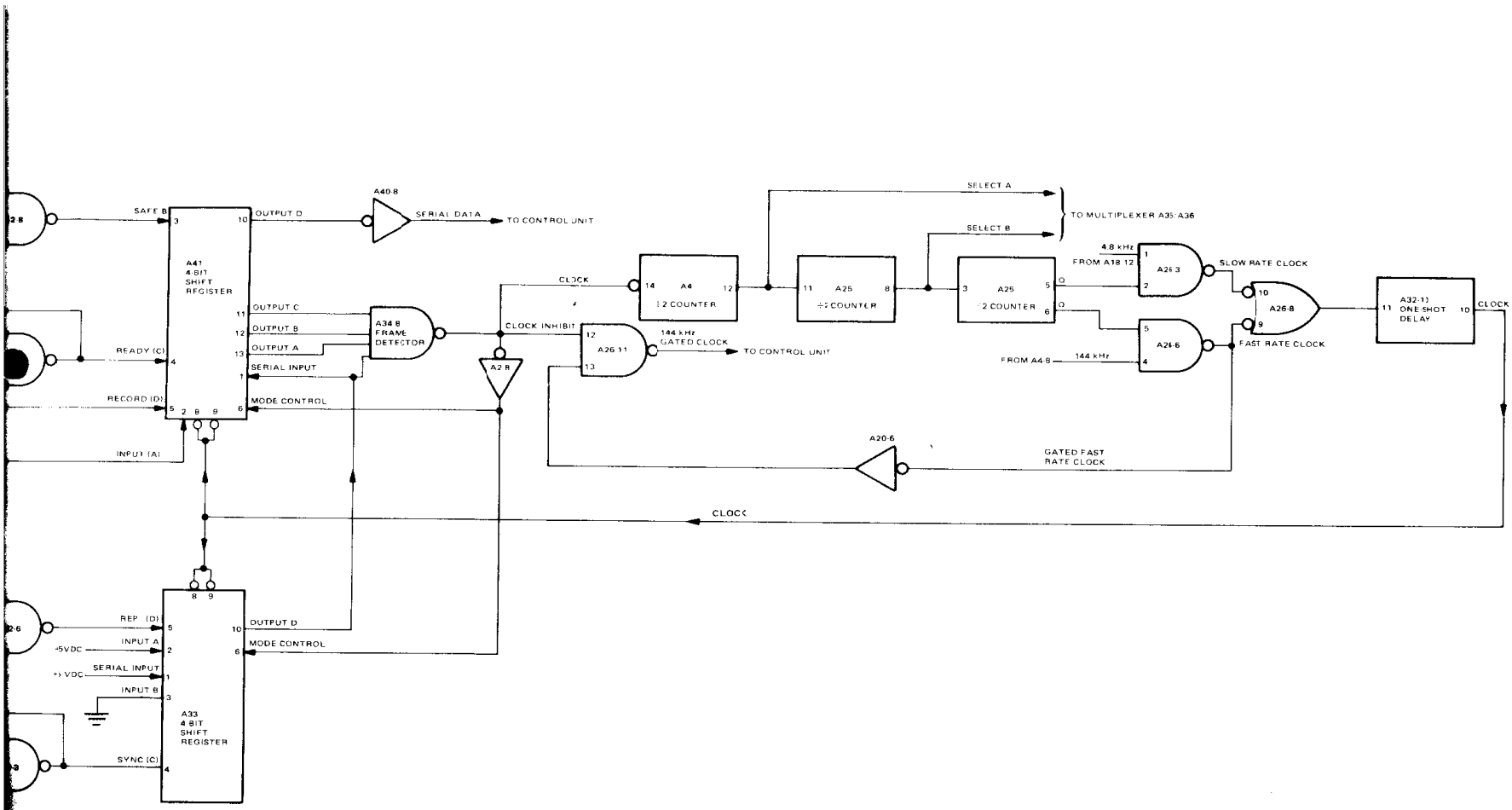
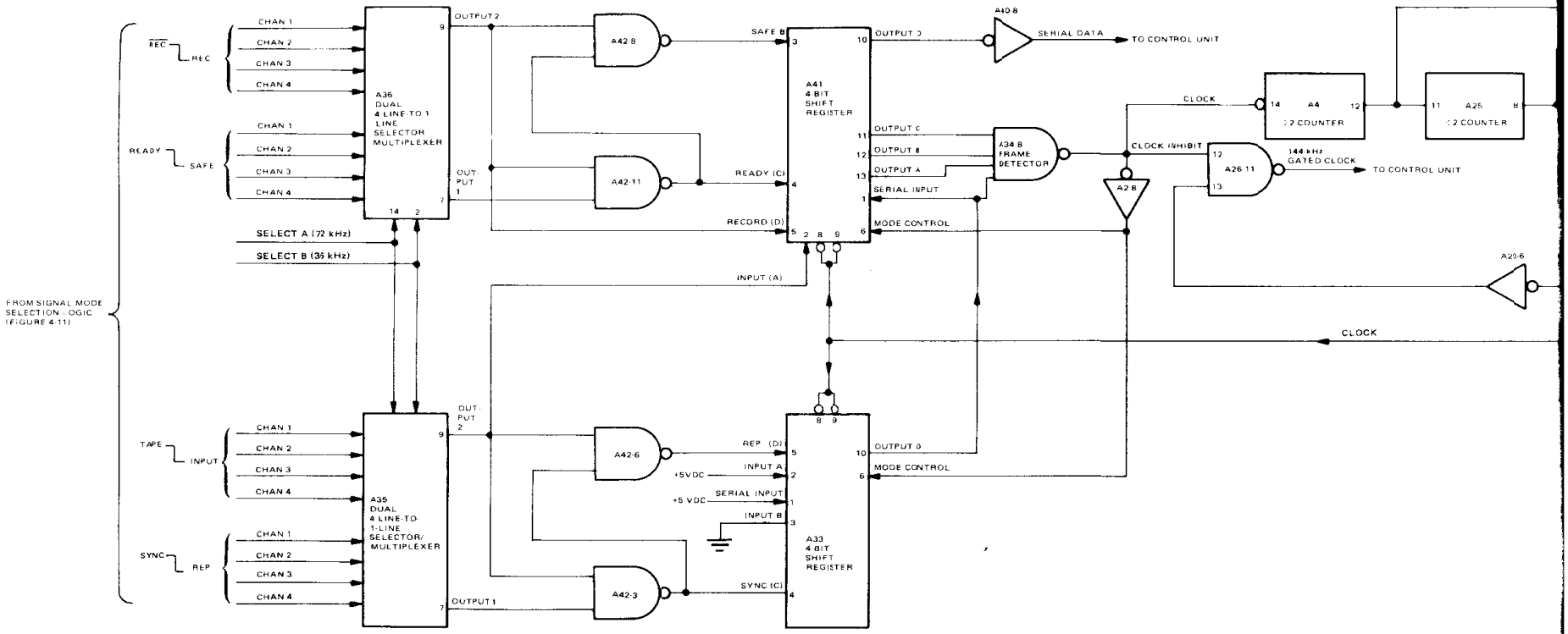


Figure 4-13. Multiplexer Simplified Block Diagram, Audio Control PWA No. 5



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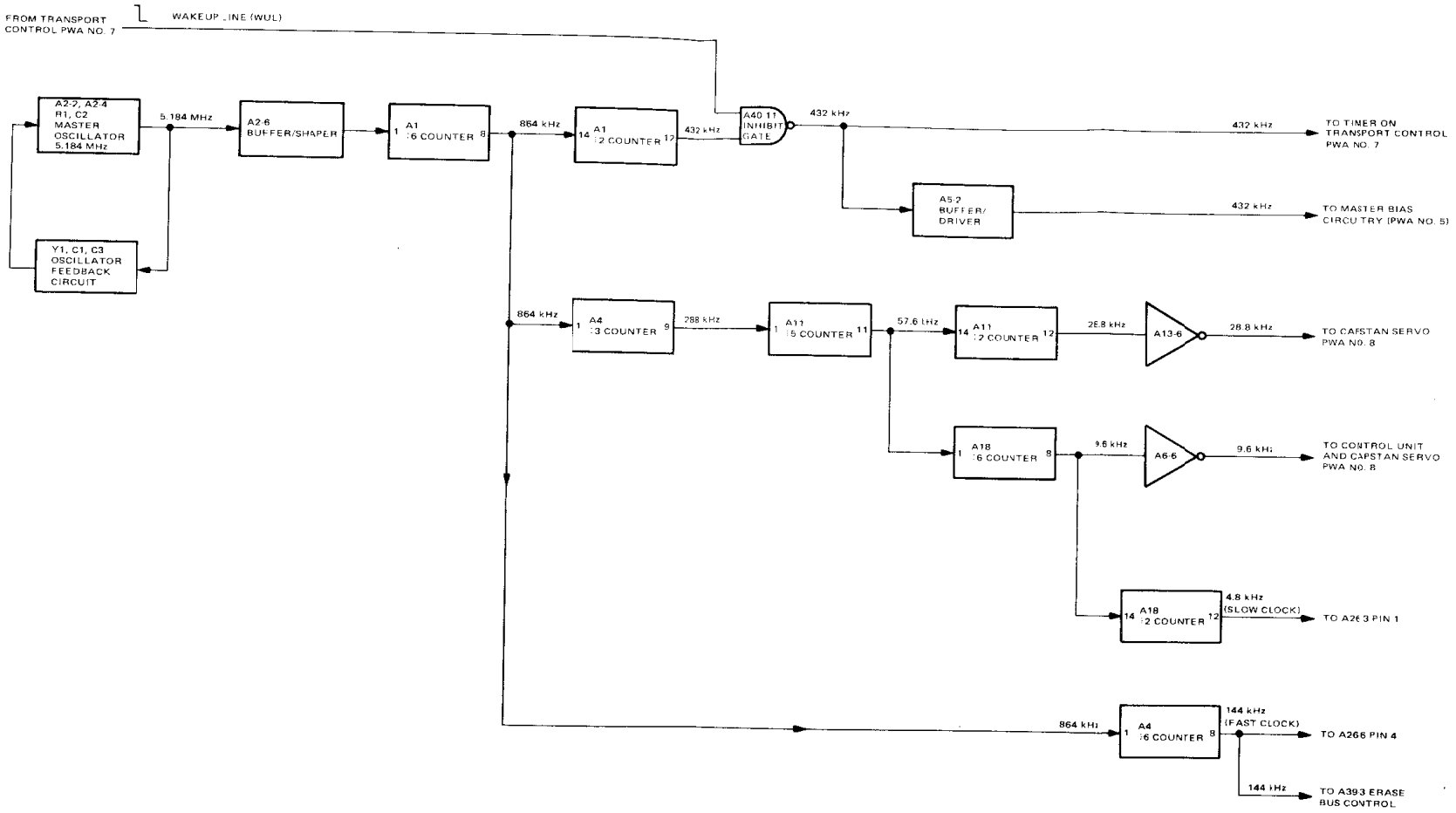


Figure 4-14. Master Oscillator and Counters, Simplified Block Diagram (PWA No. 5)

Resistor 1, in parallel with inverter A2-2, provides negative feedback and causes the inverter to try to operate as a linear amplifier. Any small disturbance at the input of A2-2 appears as an in-phase transition at the output of A2-4. This signal is applied to divider C1/C3, and the signal at the junction of C1 and C3 is fed back to the input of the amplifier through crystal Y1. Crystal Y1 acts as a very-high-Q tuned series-resonant circuit that passes only the desired frequency of 5.184 MHz. Capacitor C2 bypasses undesired harmonics and inverter A2-6 buffers the 4.184-MHz signal to provide a clean square-wave signal that is applied to the divider chain.

The 5.184-MHz signal is divided down by counters A1-8, A1-12, A4-8, A4-9, A5-2, A11-11, A11-12, A18-8, and A18-12 to provide the various signals shown on simplified block diagram Figure 4-14.

4-63. Master Erase Bus. The master erase bus circuitry accepts the 144-kHz TTL level signal from the master-oscillator counter and buffers the signal, lengthens the rise time, and provides an adjustable erase signal level that can be verified between the limits of 0 to 12 volts p-p.

As shown in Figure 4-15, the 144-kHz TTL level signal from counter A4-8 is fed through R33 to inverting CMOS amplifier A39-5/1. This amplifier serves as a buffer and ground translator which transfers the 144-kHz TTL level signal from logic ground to the audio system ground. The amplifier provides an output signal that swings between the limits of 0 and +5 Vdc. This output signal is applied across the master erase bus level control R34 which is used to establish the erase bus signal level applied to the main audio PWAs.

In the event that the 15-Vdc operating voltage, applied to the CMOS device A39, should be removed while an input signal is present, R33 will limit the input current and prevent the device from being damaged.

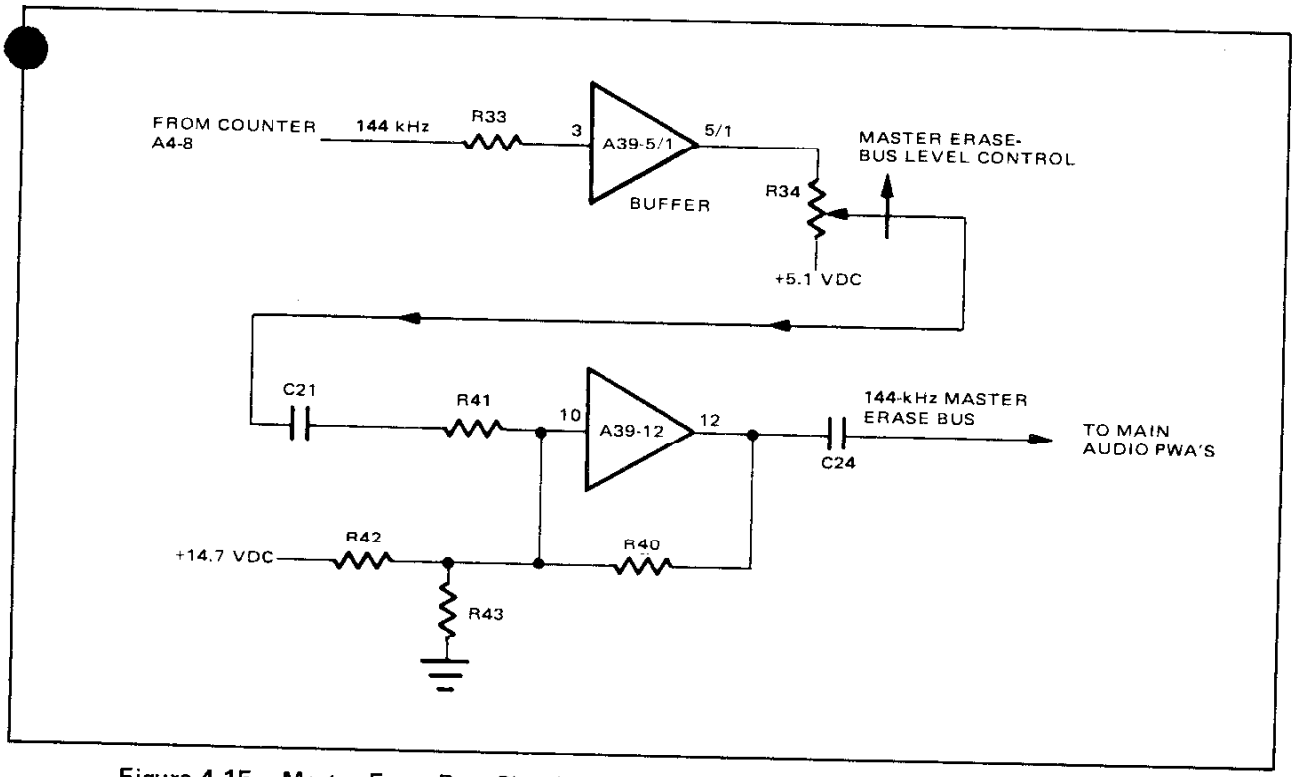


Figure 4-15. Master Erase Bus, Simplified Schematic Diagram, Audio Control PWA No. 5

The signal level selected by R34 is ac-coupled through C21 and through R41 to inverting amplifier A39-12 with feedback provided by R40. This amplifier has a gain of 3 and also serves to reduce the signal rise time which minimizes radiation into adjacent circuitry. The input of the amplifier is biased to a 7.5-Vdc level by voltage divider R42 and R43, which causes the output to be at a 7.5-Vdc nominal level and the amplifier to operate in the center of its linear range. The output signal level at pin 12 of A39 can be varied from 0 to 12 volts p-p by adjustment of master erase bus level control R34. This signal is ac-coupled through C21 and routed to main audio PWAs No. 1, 2, 3, and 4.

4-64. Master Bias Bus. The master bias bus circuitry accepts the 432-kHz TTL level signal from the master oscillator counter and buffers the signal, reduces the rise time, and provides four adjustable bias signal levels that are individually selected by a speed select logic circuit.

As shown in Figure 4-16, the 432-kHz TTL level signal from counter A1-12 is buffered and referenced to audio ground by open collector buffer/driver A5-2. The signal is applied to the junction of a voltage divider consisting of R54 and the bias level adjustment controls R3 through R6.

The other end of the adjustment controls are connected (through switch S1 and a jumper array) to the output of a 1-out-of-4 decoder speed-select logic circuit consisting of quad NAND gate A3 and inverters A2-10 and A2-12. The speed select A and B signal (SSA and SSB) in the form of a 2-bit binary encoded signal from the transport speed select switch is applied to the input of the decoder. Depending on the speed selected, one of the NAND gates (A3) is enabled, and provides a ground return (low) for one of the bias level adjustment controls. Jumper plugs J1 through J4 are used to program the recorder for 2 or 4 speed operation as shown in Table 4-6.

4-65. Two-Speed Operation. The simplified schematic (Figure 4-16) shows jumper plug connections for two-speed (7.5 and 15 in/s) operation. Switch S1 provides operational flexibility by permitting selection of either of two preset bias levels for each speed. Switch S1 in the Equalization I position enables potentiometers R4 and R6, and the switch in the Equalization II position enables potentiometers R3 and R5 when the associated speed is selected.

Depending on the speed selected, the associated bias level adjustment control is adjusted to the desired 432-kHz signal level, and this level is ac-coupled through C22 and through R39 to inverting amplifier A39-3/8 with feedback provided by R55. The amplifier has a gain of approximately 2, and reduces the signal rise time to minimize radiation into adjacent circuitry. The input to the amplifier is biased to a 7.5-Vdc level by voltage divider R39 and R37 which causes the output signal to be at a 7.5-Vdc nominal level and the amplifier to operate in the center of its linear range. The output signal level at pin 13/8 of A39 can be varied from 0 to 8.0 volts p-p by adjustment of a bias level adjustment control. The output signal is ac-coupled through C25 and routed to main audio PWAs No. 1, 2, 3, and 4.

4-66. Four-Speed Operation. For four-speed operation, jumper plugs J1 through J4 are positioned as shown in Table 4-6. Note that for four-speed operation, switch S1 should remain in the "I" position, as one bias level adjustment control is used for each speed, as shown in the table.

4-67. Illegal Speed Detector. If jumpers J1 through J4 are positioned for two-speed operation (Table 4-6) and one of the other non-programmed speeds is selected by operation of the transport speed select switch, the illegal speed line (ISL) will become active (low) and cause the transport to become inactive in play and record modes at that speed. (The ISL line also becomes active if no jumpers are installed.)

The illegal speed detector circuitry consists of diodes CR1 through CR5, capacitor C5, and transistor Q1. When a speed is selected for which jumpers J1 through J4 have been correctly placed, one diode (CR1 through CR4) will conduct and its anode will be one diode drop (0.7 volt) above the saturated output of A3. This prevents Q1 from turning on and generating an ISL command because of the voltage drop across CR5.

If an incorrect speed is selected, one or more of diodes CR1 through CR4 will open-circuit and

diode CR5 will conduct and charge C5. After C5 is charged, Q1 will turn on and generate a low ISL command. In addition to causing the transport to become inoperative, the low from the collector of Q1 also causes the input/input and tape/tape output lines to both become high. This causes the audio output lines from each audio PWA to become muted.

4-68. Main Audio Functional Description

The main audio consists of up to four identical main audio PWAs and their parameter determining network (PADNET) PWAs. One main audio PWA and its associated PADNET PWA comprise the main audio for each record/reproduce channel. The main audio for channels 1 through 4 is located on PWA No. 1 through PWA No. 4, respectively. The main audio PWA and its associated PADNET PWA contain the erase, record, reproduce, and audio output circuits for one audio channel. Additionally, control logic circuitry located on the main audio board and PADNET provides bias and erase ramping control, pick-up record capability (PURC), tape-speed decoding, and other timing and control signals required by the main audio for that channel. The speed-dependent record and reproduce equalization networks, record and reproduce level presets, bias normalization preset, and tape-speed decoding logic are contained on the PADNET assembly which plugs into the main audio board. The PADNET is capable of being adjusted to provideo for record and reproduce equalization and can accommodate all equalization standards at any one of the selected transport tape speeds (30, 15, 7.5 or 3.75 in/s). Figure 4-17 is a simplified block diagram of the main audio for one record/reproduce channel.

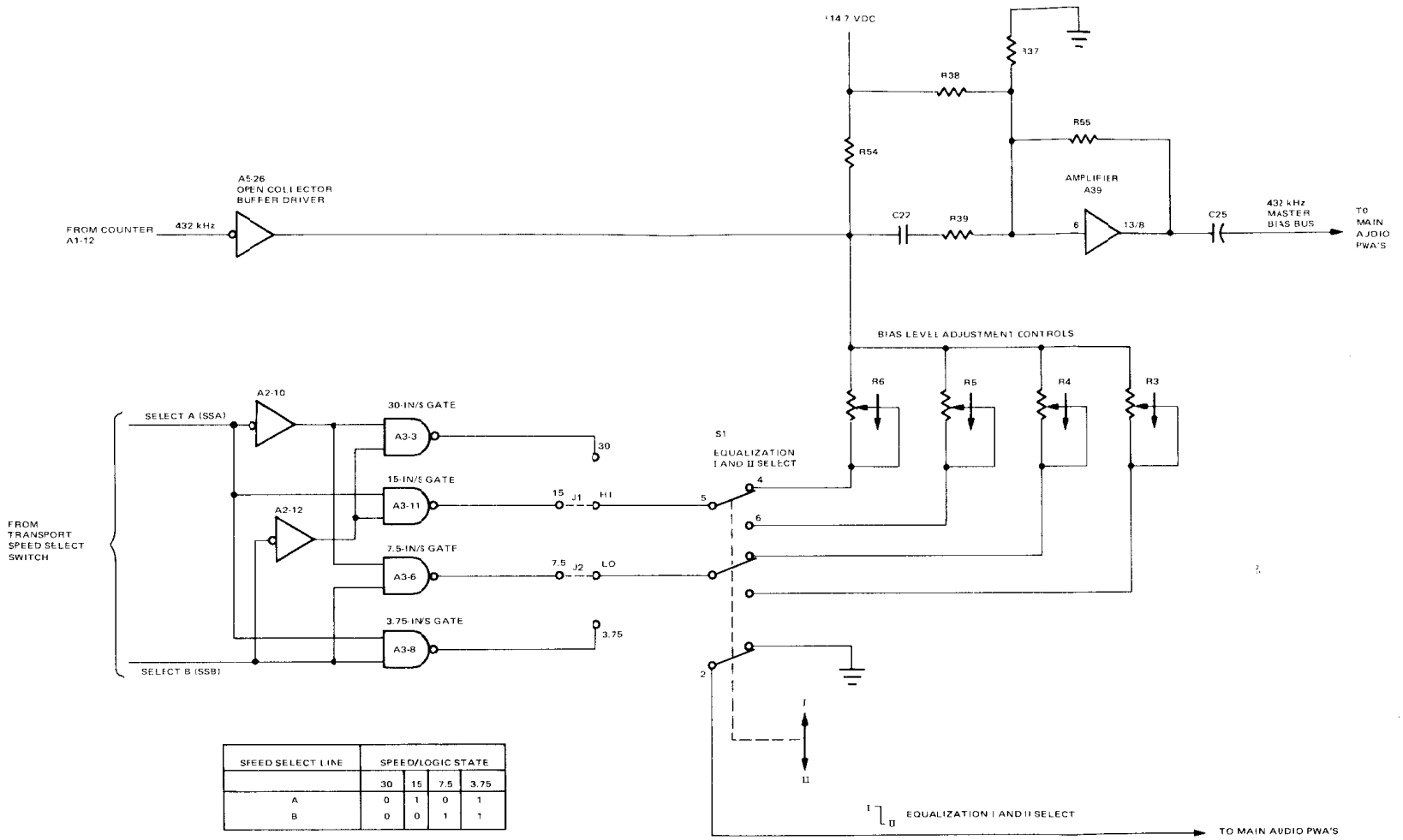
The record circuits receive the system audio input and 432-kHz bias, and provide equalization of the received audio signal to match the required recording equalization at the selected tape speed and/or equalization standard. The record circuits also combine the equalized signal with the 432-kHz bias to provide the drive signal to the record head on the tape transport.

The reproduce circuits receive playback audio from the reproduce head or sel sync audio from the record head, as selected by the operator. The reproduce circuits provide the required playback equalization of either tape signal to match the selected tape speed and/or equalization standard. The selected tape signal is sent to the output amplifier circuits. Additionally, the unequalized sel sync signal is available at the card-edge connector.

The audio output circuits receive the tape and input signals from the reproduce circuits or input circuits, respectively, and provide selection and buffering of the tape or input signals to the input/output module.

The erase circuit receives the 144-kHz erase signal and provides buffering of the erase signal to the erase head via the erase amplifier. The output of the erase amplifier is fed to the erase head via the erase reed relay. The erase reed relay is normally open. When the safe/record signal is low (record) the erase reed relay is energized and the normally-open contacts are closed to provide a current path for the erase signal to the erase head. The control signal for the erase reed relay is provided via the control logic on the main audio board.

The control logic receives the safe/record, tape speed, and tape/input selection signals and generates the control signals to the circuits on the audio main and PADNET assemblies. The control logic provides the tape or input switching signals to the audio output circuits, decoded transport tape-speed selected signals to the record and reproduce circuits, and ramping and control signals to the record circuits. The control logic also contains the pick-up recording capability (PURC) circuits. The PURC circuits eliminate overlaps and erased gaps in recordings when inserting (dubbing) new material within previously-recorded programs. In a recorder system without PURC, initiating the record mode energizes the erase and record heads simultaneously. Since there is a physical distance between the erase head and the record head, a period of over-recording on the unerased tape occurs and, when the dubbing is terminated, an erased gap is left in the program. The length of over-recording and the erased gap on the tape is determined by the distance between the erase and record heads and the transport tape speed.



SPEED SELECT LINE	SPEED/LOGIC STATE			
	30	15	7.5	3.75
A	0	1	0	1
B	0	0	1	1

Figure 4-16. Master Bias Bus, Two-Speed Simplified Schematic (PWA No. 5)

Table 4-6. Speed Jumper Placement and Bias Switch Setting, Audio Control PWA No. 5

2-SPEED OPERATION			
SPEED	SET JUMPERS TO DESIRED SPEED	MASTER BIAS (ADJUST S1 POSITION I)	MASTER BIAS (ADJUST S1 POSITION II)
HI SPEED LO SPEED	J1 – 30, 15, 7.5 J2 – 15, 7.5, 3.75	R6 R4	R5 R3
NOTE: J3 and J4 to be jumpered to the S (store) positions.			

4-SPEED OPERATION	
JUMPER	MASTER BIAS (ADJUST S1 POSITION I ONLY)
J1 – 30 J3 – 15 J2 – 7.5 J4 – 3.75	R6 R5 R4 R3

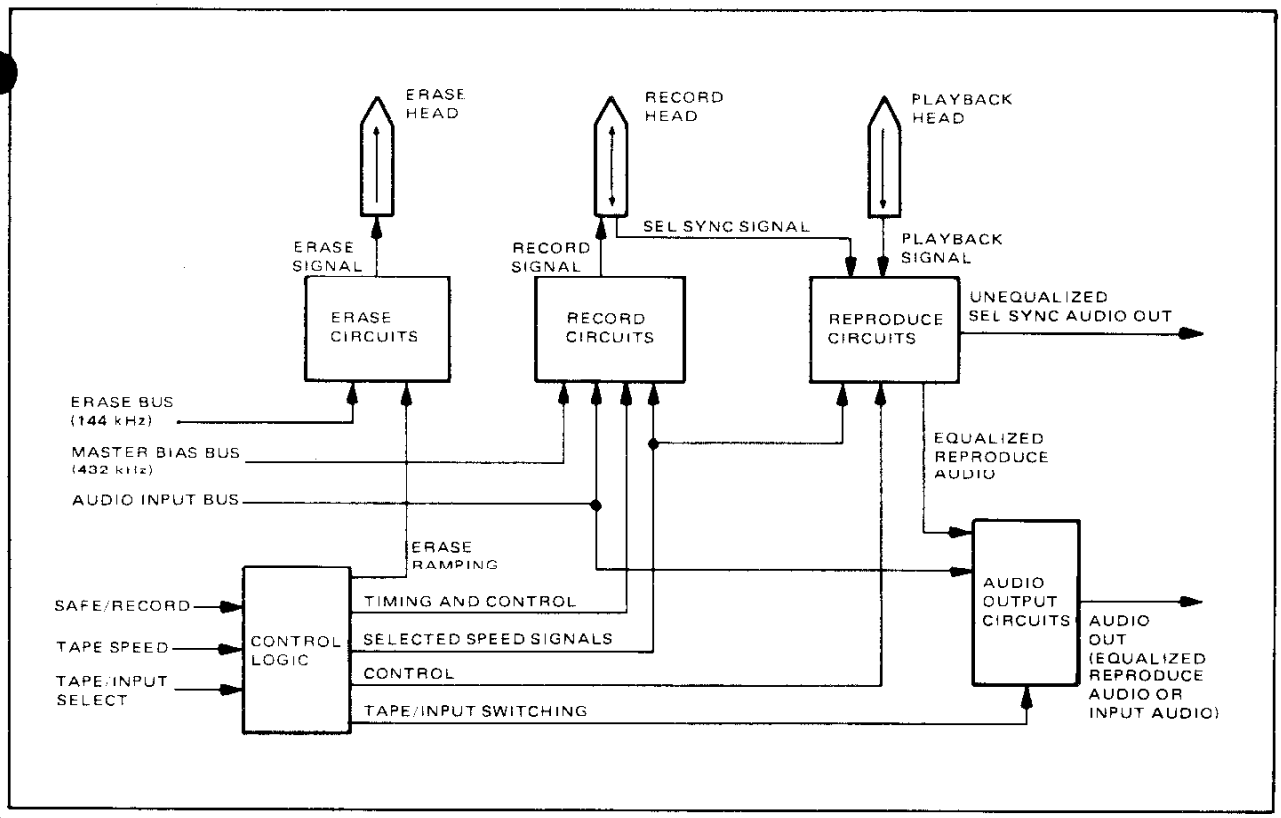


Figure 4-17. Main Audio Simplified Block Diagram

The PURC circuits eliminate the over-recording and erase gap by generating a delay between the time that the erase ramping is initiated and the bias/audio ramping is initiated. When the recorder/reproducer goes into the record mode, the erase ramp up is initiated first; then, after a delay determined by the selected tape operating speed, the bias/audio ramp up is initiated. When the recorder/reproducer is switched out of the record mode, the erase ramp down is initiated first; then, after a delay determined by the selected tape operating speed, the bias/audio ramp down is initiated. In this manner, the effect of the physical difference between the erase and record heads is cancelled and the overlap and gap are eliminated from the dubbed portion of the recording.

4-69. Main Audio Circuit Details

Each of the four channels of the main audio is identical. The main audio circuits for channels 1 through 4 are located on PWA No. 1 through PWA No. 4, respectively for each channel. The following paragraphs describe the main audio circuits that comprise a single channel. Each channel contains one audio main board and plug-in PADNET assembly. Drawing 4840378 is the schematic diagram for the audio main board, and drawing 4840379 is the schematic diagram for the PADNET assembly.

4-70. Control Logic. The control logic generates ramping, timing, and switching signals for the main audio. As shown in Figure 4-18, the control logic contains the ramping, PURC delay, tape-speed decode, and output amplifier switching logic.

4-71. Speed Decode Logic. The speed decode logic is contained on the PADNET assembly. As shown in Figure 4-18, the speed decode logic receives the selected speed signals, SSA and SSB, from the transport unit speed selector and decodes the four possible combinations of the two signals to provide selection of networks within the PADNET assembly. These speed signals are active low. When SSA and SSB are both low (30 in/s), the output of NAND gate A2-11 goes low and NAND gates A2-3, A2-4, and A2-10 are high. In a similar manner, each of the NAND gates provides a low signal which corresponds to a selected tape speed as determined by the selected speed signals from the tape transport. The individual selected speed signals (30, 15, 7.5, and 3.75 in/s) are used to gate different timing networks in the PURC circuit. The decoded 30 in/s and 15 in/s are also used in the reproduce equalizer circuits to gate additional compensation into the equalization networks. The four decoded speed signals are used on the PADNET for selection of high and low speed equalization network via jumpers P1 and P2 and J1 and J2, respectively.

The standard PADNET assembly provides a choice of any two standard operating speeds that are compensated by the high and low speed equalization networks on the PADNET. The operating tape speeds are selected by jumpers on the PADNET. The high-speed equalization circuits may be enabled at 30, 15, and 7.5 in/s. The low-speed equalization circuits may be enabled at 15, 7.5, and 3.75 in/s. If the tape operating speed selected at the tape transport does not correspond to the speed selected on the PADNET to enable the high or low speed equalization, the recorder/reproducer is inhibited from operating in either play or record modes and the lockout indicator on the control unit is lit. The lockout signal, ISL, is generated by a NAND gate consisting of Q14 and CR8 through CR10. The decoded high- and low-speed equalization network selection signals provide the inputs to NAND gate Q14/CR8-10. If neither high- nor low-speed selected signals are low (0 Vdc), the output of NAND gate Q14/CR8-CR10 goes low denoting that a tape speed has been selected at the transport which does not correspond to a selected speed on the PADNET. All logic integrated circuits (ICs) on the PADNET are CMOS-type circuits; therefore, the logic levels in the circuits range from +15 Vdc (high) to 0 Vdc (low).

4-72. Erase Ramping. The turn on and turn off of the erase signal is controlled by the SAFE/REC signal from the audio control PWA No. 5. When the channel is not in the record mode, the SAFE/REC signal is high. The SAFE/REC signal, through resistor R42, is applied to a summing point at the inverting input of erase ramping amplifier A7-14. Erase ramping amplifier A7-14 and ramping network C36/VR1/VR2/CR11/C38/R44 generate the ramp and control signals for the erase ramping switch Q14 and erase head relay driver Q17/VR5. The ramping network provides feedback from the

output of the erase ramping amplifier A7-14 back to the summing point at the inverting input of the amplifier. When the SAFE/REC signal is high (not record mode), the output of the erase ramping amplifier A7-14 is nominally −10 Vdc. The −10 Vdc, via the PADNET, is applied to erase head relay driver Q17/VR5. The −10 Vdc biases the transistor off, which keeps relay K2 de-energized. The −10 Vdc, via the ramping network, enables a negative bias to be applied through resistor R70 and diode CR17 to the base of erase ramping switch Q14. Transistor Q14 operates in the inverted mode and conducts when the negative bias is applied, thereby shunting the 144-kHz erase signal, at the input to erase amplifier A10/Q18/Q19, to ground.

When the channel is switched into the record mode, the SAFE/REC signal goes low. When the SAFE/REC signal goes low, the low-going input supplied to the inverting input of erase ramping amplifier A7-14 causes the output of the amplifier to start rising toward the +10-Vdc level. The output of erase ramping amplifier A7-14 is fed back to the summing point at the inverting input and to erase switch Q14 via the ramping network. The ramping network, together with erase ramping amplifier A7, forms an active integrating amplifier that generates an erase ramping signal that is applied to the base of Q14. This signal is used to shape the 144-kHz erase signal applied to the emitter of Q14. The controlled base drive produces an amplitude-controlled ramped 144-kHz signal which is applied to erase amplifier A10/Q18/Q19. The erase ramping signal also controls the timing for energizing erase head relay K2 via erase head relay driver Q17/VR5. When the channel is switched out of the record mode, the SAFE/REC signal goes high. The positive-going input to the summing point at the inverting input of erase ramping amplifier A7-14 causes the output of the integrating amplifier formed by the erase ramping amplifier A7-14 and the ramping network to swing towards negative 10 Vdc. The negative-going ramp generated by the integrating amplifier provides the turn-off ramp for the 144-kHz erase signal to the input of the erase amplifier via transistor switch Q14. The negative-going ramp also provides the timing to de-energize erase head relay K2 via erase head relay driver Q17/VR5.

4-73. Record Ramping and PURC Logic. The record ramping and pick-up record capability (PURC) logic generates the appropriate ramping signals for the controlled ramping up and down of the bias to the record circuits and for timing of the PURC delays. All control sequences are initiated when the status of the channel SAFE/REC signal, generated by the audio control PWA, changes. Figure 4-19 is a timing diagram of the ramping and PURC delay signals.

As discussed previously, operational amplifier A7-14 is connected to form an active integrator to generate the erase ramping control for erase ramping switch Q14, and to provide the control for the erase head relay K2 via erase head relay driver Q17/VR5. Operational amplifier A7-8 is connected to form an active integrator that provides the required ramping control to bias ramping switch Q7, and control the operating sequence of the record head reed relay K1, sel sync shunt switch Q6, record audio switch Q9, and bias command status switch Q8/Q10. Operational amplifier A7-1 forms an active integrator which, in conjunction with hysteresis switch A7-7 and timing selection FET Q8 through Q11, provides the selected delay timing for PURC operation.

When the recorder/reproducer goes into the record mode, the SAFE/REC signal goes low and turns on ±15V switch Q7 which switches the −15 Vdc at the input to PURC delay amplifier A7-1 to +15 Vdc via a selectable resistor network. Jumper plug P3 is used to select PURC operation when the recorder is switched into record mode. When the jumper plug is in the PURC position, +15 Vdc from the ±15V switch Q7 is supplied to the resistor network comprised of four resistors, R36 through R39. One of the four resistors is selected by the decoded speed select signals specifying the tape operating speed and supplies a constant current, as determined by the selected resistor, to the input of the PURC delay amplifier A7-1. When the jumper is in the NORM (PURC disabled) position, positive 15 Vdc from the 15-Vdc switch Q7 is supplied to PURC delay amplifier A7-1 through resistor R30 independent of the selected tape operating speed. Resistor R30 or resistors R36 through R39, depending on whether PURC operation is selected via jumper plug P3, provide different delay times in conjunction with the integrating

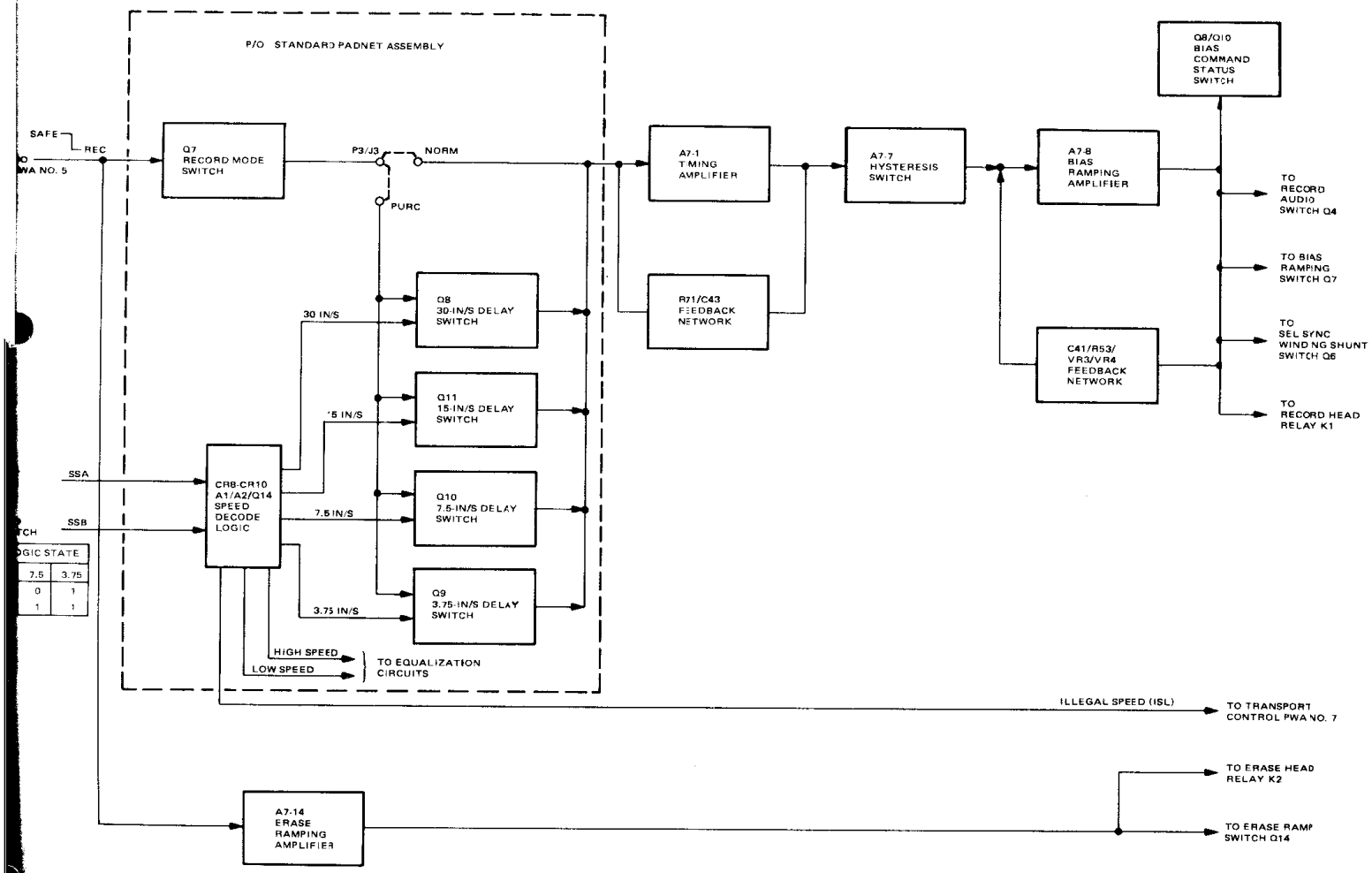
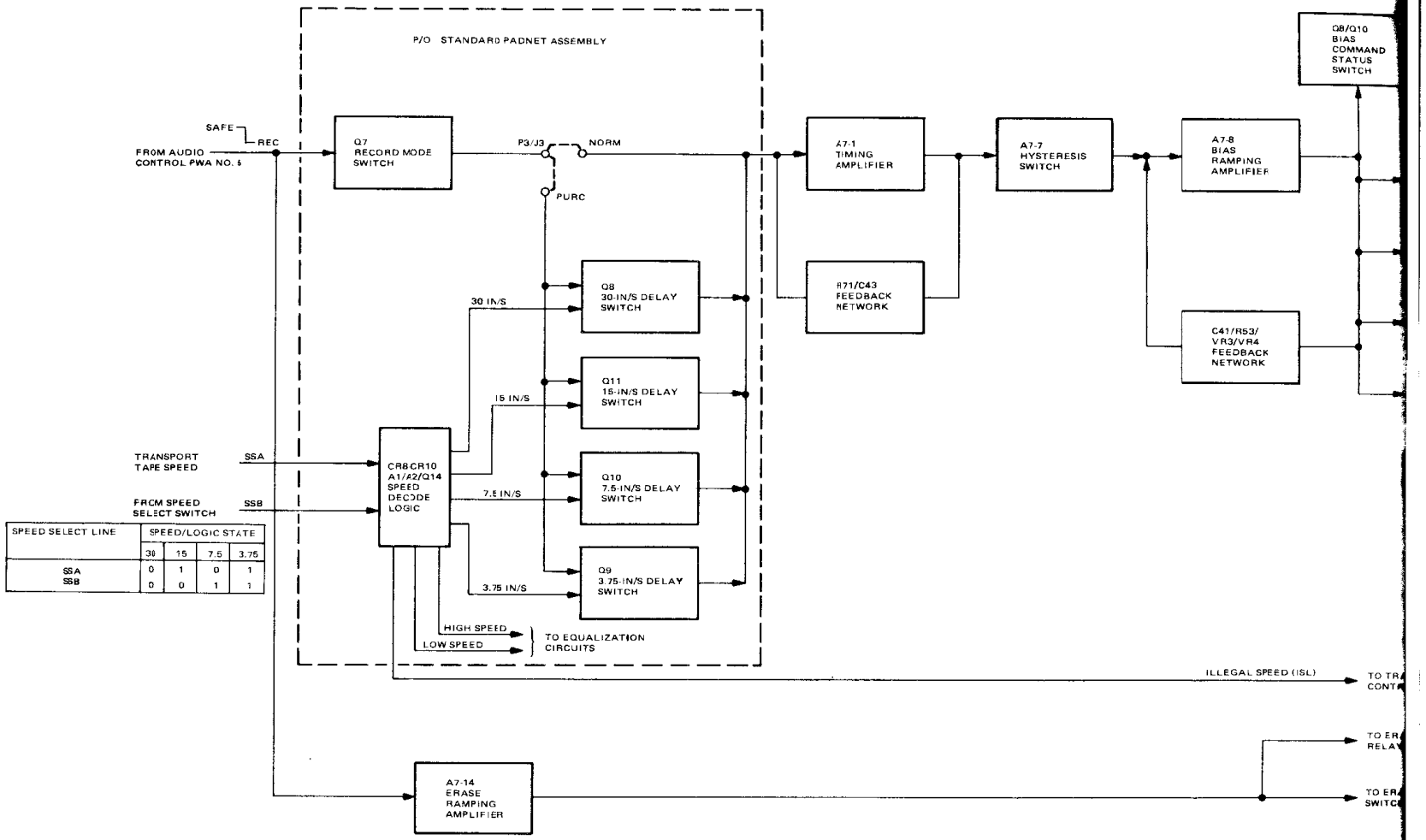


Figure 4-18. Main Audio Control Logic, Simplified Block Diagram



SPEED SELECT LINE	SPEED/LOGIC STATE			
	30	15	7.5	3.75
SSA	0	1	0	1
SSB	0	0	1	1

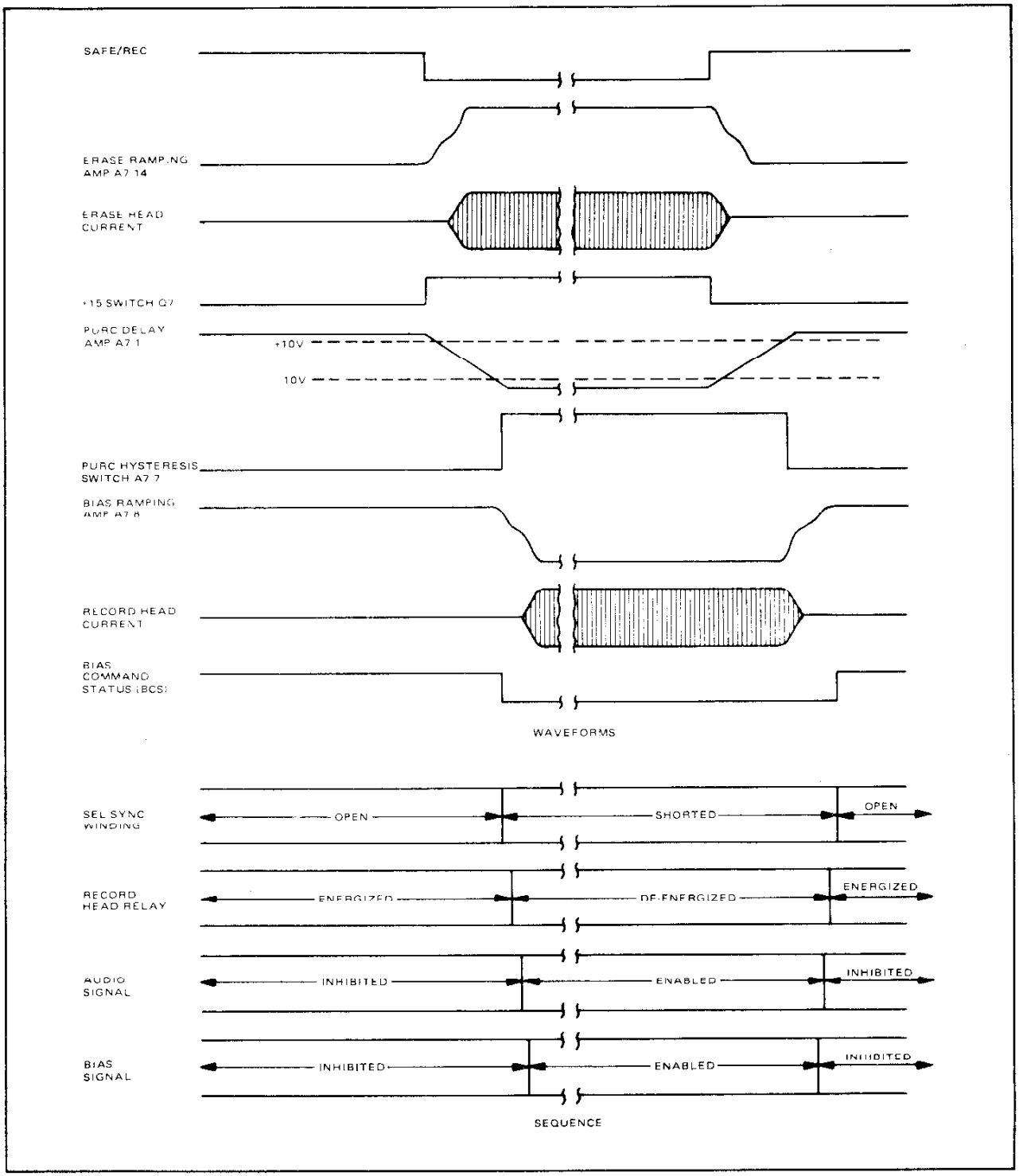


Figure 4-19. Record Ramping and PURC Delay Timing

amplifier formed by PURC delay time amplifier A7-1 with resistor R71 and capacitor C43. Resistors R36 through R39 are individually selected by FET switches Q8 through Q11 by the decoded speed selected signals. When the corresponding selected tape speed signal goes low, the associated FET switch is turned on and provides a current path through the resistor to the input of PURC delay amplifier A7-1.

When the recorder/reproducer is switched into the record mode, the SAFE/REC signal goes low and switches +15 Vdc, via +15V switch Q7 and resistor network R30/R36-R39, to PURC delay amplifier A7-1. PURC delay amplifier A7-1 generates a negative-going ramp. The slope of the ramp is determined by the selected resistor in resistor network R30/R36-R39 and C43/R71. The ramp from PURC delay amplifier A7-1 goes to the PURC hysteresis switch A7-7. The PURC hysteresis switch A7-7 is a comparator, which compares the level of the delay ramp with one of two levels. The two comparison levels are derived by a positive feedback network that decreases the output level of the PURC hysteresis switch A7-7 by approximately two-thirds. When the recorder/reproducer is in the safe mode (SAFE/REC signal is high), the output of the PURC hysteresis switch A7-7 is low (approximately −15 Vdc). The comparison reference level fed back to the input of the comparator is approximately −10 Vdc during the safe mode and remains at −10 Vdc until the level of the negative-going ramp exceeds −10 Vdc, at which time the output of PURC hysteresis switch A7-7 will go to +15 Vdc. The slope of the ramp, therefore, determines the difference between the time that the SAFE/REC signal goes low and the time that the output of PURC hysteresis switch A7-7 goes high.

As long as the recorder/reproducer remains in the record mode (SAFE/REC signal low), the output of the PURC hysteresis switch remains high (+15 Vdc) and a new reference level of +10 Vdc is fed back to the input of the comparator. The positive-going edge of the signal from PURC hysteresis switch A7-7 initiates the bias ramp, which controls the timing of record signals. The bias ramp is generated by active integrator bias-ramping amplifier A7-8. When the output of PURC hysteresis switch A7-7 goes high, a negative-going ramp voltage is generated by bias-ramping amplifier A7-8. Bias and current-limiting of the signals by electronic switches in the record circuits control the turnon and turnoff sequence of operations. As the bias ramp goes negative, the following operations occur in the order given.

1. Status switch Q8/Q10 is turned on and supplies a logic low to bias command status line — BCS.

2. Sync shunt switch Q6 is turned on and shorts the sel-sync winding on the record head.

3. Record head relay Q11/K1 is de-energized, which removes the short across the record winding of the record head.

4. FET switch Q9 is switched on and enables the audio input to record amplifier A9/Q12/Q13.

5. Bias switch transistor Q7 is ramped off and provides a corresponding ramping up of the bias input to record amplifier A9/Q12/Q13.

When the recorder/reproducer is switched out of the record mode, the SAFE/REC signal goes high and turns off 15-Vdc switch Q7. With the +15-Vdc supply to resistor network R30/R36-R39 turned off, −15 Vdc is applied to the selected input resistor which provides the current to PURC delay amplifier A7-1. With −15 Vdc at the input, PURC delay amplifier A7-1 generates a positive-going ramp from −15 Vdc to +15 Vdc. The slope of the positive-going ramp is determined by the selected resistor in resistor network R30/R36-R39 and C43/R71. Since the −15 Vdc is applied through the same resistor network as the +15 Vdc, the slope of the positive-going ramp when the recorder/reproducer is switched out of the record mode is the same as the slope of the negative-going ramp when the recorder/reproducer is switched into the record mode.

The positive-going ramp goes to hysteresis switch A7-7. During record, the output of hysteresis switch A7-7 is +15 Vdc. Therefore, the comparison reference level for hysteresis switch A7-7 is shifted to +10 Vdc in the same manner that the −10-Vdc reference was generated going into record. When

the level of the positive-going ramp exceeds +10 Vdc, the output of PURC hysteresis switch A7-7 goes rapidly low and initiates a positive-going ramp, which is generated by bias ramping amplifier A7-8. As the bias ramp goes positive, the following operations occur in the order given.

1. Bias switch transistor Q7 is ramped on, which ramps down the bias input to record amplifier A9/Q12/Q13, thereby removing the bias signal to the amplifier.

2. FET switch Q9 is biased off, which removes the audio input to record amplifier A9/Q12/Q13.

3. Record head relay Q11/K1 is energized, thereby shunting the record head windings.

4. Sync shunt switch Q6 is turned off and opens the short across the sel-sync windings of the record head.

5. Status switch Q8/Q10 is turned off, removing the logic low from the bias command status line (BCS), which allows bias command status line BCS to go high.

4-74. Record Circuits. As shown in Figure 4-20, the main part of record equalization is performed by amplifier A6-6 in conjunction with an active differentiator formed by amplifier A5-6, input capacitor C5, and feedback resistor R40.

The audio input signal is split into three paths. The first path is via R39 to the summing node (pin 2 of A6-6). The second path is to the input network C5/R41 of the active differentiator. The third path is to the summing node of A6-6 via C13/R54/R55, with alternate paths selected by S1 and FET switches Q12 and Q13 for high- and low-speed switching equalization, respectively.

The output from the active differentiator A5-6 will, for a constant amplitude signal, rise 6 dB per octave with increasing frequency. Time constant components C5/R41 limit the maximum frequency of the rise. This output signal is then applied to equalizer potentiometer controls R15 and R18, which are the main high-frequency equalizer controls for high-speed and low-speed operation, respectively. The setting of these equalizer controls determines how much of the differentiated signal is summed with the direct signal, via R39, supplied to the summing node of A6-6. Selection between the output of R15 or R18 is accomplished by FET switches Q12 and Q13, respectively.

A series of switch selectable networks formed by R16/R16/C8/C9 (switched by S1-1 and S1-3 for high speed) and R19/R20/C10/C11 (switched by S1-4 and S1-6 for low speed) form additional frequency dependent feedback around A6-6 to the summing node of A6-7. Selection for high or low speed is also accomplished by FET switches Q12 and Q13.

The network formed by C13/R54/R55 and selected for high speed operation by S1-2 and for low-speed operation by S1-5, also provides separate frequency dependent preset equalization. In this instance, the network effectively appears in parallel with R39.

The networks switched by S1-1 and S1-4 provide mid- to high-frequency shelf down for high and low speeds, respectively. Switches S1-3 and S1-6 provide selectable constant current or 3,180-μs low-frequency pre-emphasis for high and low speeds, respectively. Switches S1-2 and S1-5 provide a mid- to high-frequency shelf up for high and low speeds, respectively. Table 4-7 is a list of the switch settings for preset equalization network settings.

The equalized audio from amplifier A6 goes to record gain control R12 on the PADNET assembly. The audio from the gain control potentiometer R12 (REC GAIN) on the PADNET assembly goes through R47 back to the audio main board to FET switch Q9, which gates the audio to the summing junction of amplifier A9 in the recording amplifier. FET switch Q9 gates the audio under control of audio switch control network R62/CR9/C56, which receives a control signal from bias ramping control amplifier A7-8 in the control logic. The recording amplifier A9/Q12/Q13 is a wide-band voltage amplifier consisting of operational amplifier A9 and a complementary driver output amplifier Q12/Q13.

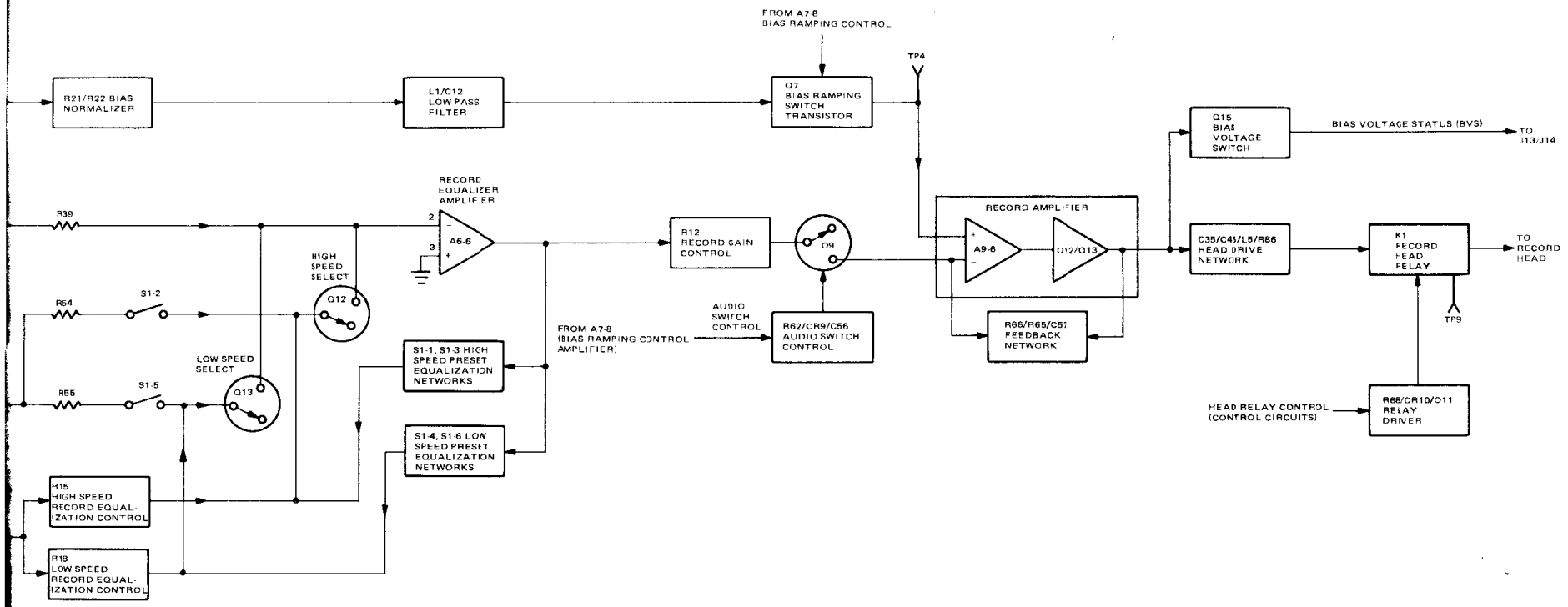


Figure 4-20. Audio Record Circuits, Simplified Block Diagram

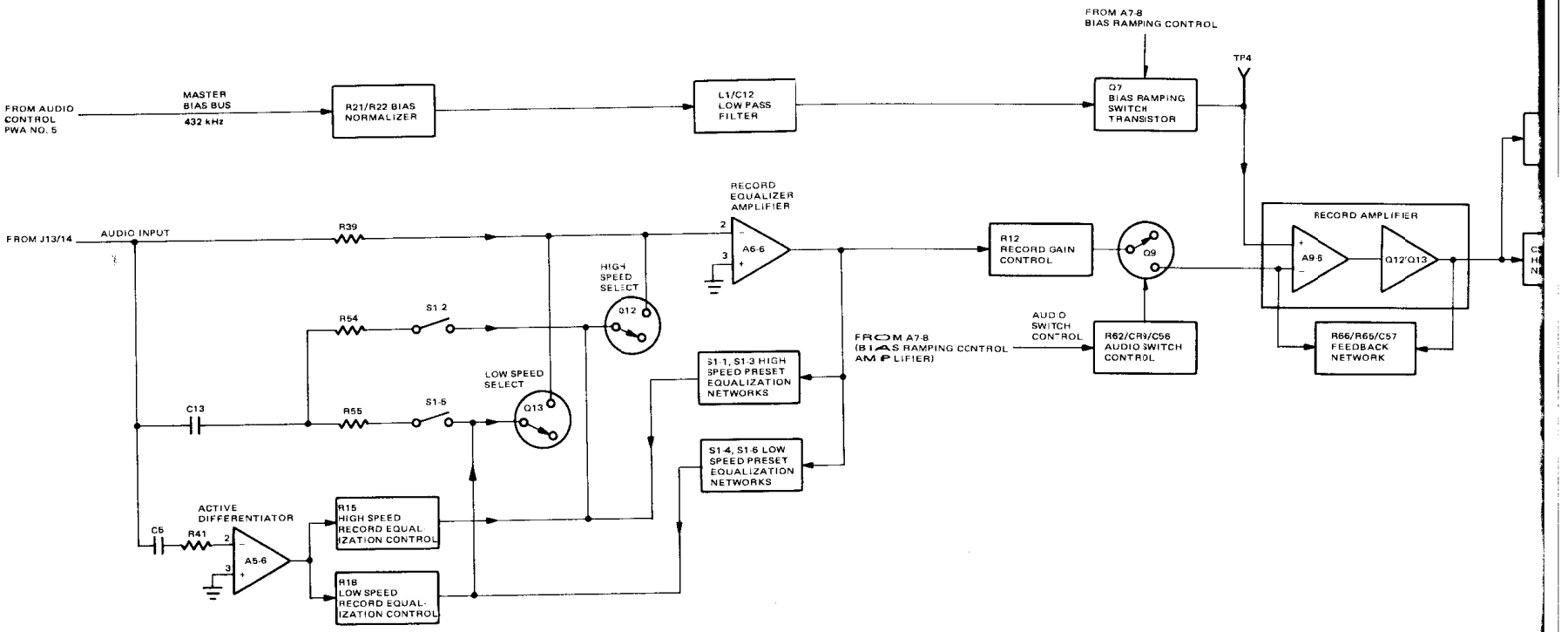

FROM AUDIO CONTROL PWA NO. 5
MASTER BIAS BUS
432 kHz
R21/R22 BIAS NORMALIZER
L1/C12 LOW PASS FILTER
FROM A7-8 BIAS RAMPING CONTROL
Q7 BIAS RAMPING SWITCH TRANSISTOR
TP4
FROM J13/14
AUDIO INPUT
R39
RECORD EQUALIZER AMPLIFIER
A6-6
HIGH SPEED SELECT
Q12
R54
S1-2
LOW SPEED SELECT
Q13
C13
R55
S1-6
S1-1, S1-3 HIGH SPEED PRESET EQUALIZATION NETWORKS
S1-4, S1-6 LOW SPEED PRESET EQUALIZATION NETWORKS
ACTIVE DIFFERENTIATOR
C6
R41
A5-6
R15 HIGH SPEED RECORD EQUALIZATION CONTROL
R18 LOW SPEED RECORD EQUALIZATION CONTROL
R12 RECORD GAIN CONTROL
Q9
FROM A7-8 (BIAS RAMPING CONTROL AMPLIFIER)
AUDIO SWITCH CONTROL
R62/CR9/C56 AUDIO SWITCH CONTROL
RECORD AMPLIFIER
A9-5
Q12'Q13
R66/R65/C57 FEEDBACK NETWORK

Table 4-7. Preset Equalization Network Settings

PRESET RECORD EQUALIZATION		
S1-1 S1-2 S1-3	SHELF DOWN SHELF UP 3180/∞	HI SPEED
S1-4 S1-5 S1-6	SHELF DOWN SHELF UP 3180/∞	LO SPEED

Shelf up or shelf down will be selected with the switch in the "ON" position. Infinity (∞), no low frequency boost will be selected with the switch "ON" and low frequency boost (3180-μs time constant) with the switch "OFF."

The 432-kHz bias signal is received at the main audio PWA, where it is routed to the bias normalizing and filtering circuits on the PADNET. Bias normalizing resistor R21/R22 provides level setting of the received 432 kHz from the master bias bus via BIAS NORM potentiometer R21. The level normalized bias signal is then filtered by bandpass filter L1/C12 on the PADNET. The filtered bias is sent to bias ramping switch transistor Q7 on the main audio PWA. Bias ramping switch transistor Q7 operates in the inverted mode and, under control of the bias ramp control signal from ramping amplifier A7-8 in the control logic, provides ramping of the bias signal to operational amplifier A9 where it is effectively added to the audio which is applied to the inverting input. The combined audio/bias signal from operational amplifier A9 is sent to complementary driver output amplifier Q12/Q13, which buffers the signal to head drive network C30/C45/L5/R86. Additionally, part of the signal from operational amplifier A9 is also sent to bias voltage switch Q15 and to feedback network R66/R65/C67. This network (R66/R65/C67) provides negative feedback around the record amplifier A9/Q12/Q13. Bias voltage present on the output of the record amplifier also provides the control signal to the base of transistor Q15 which, when bias is present, will provide a low on the bias voltage status (BVS) line from the audio main board.

The output of the record amplifier goes to the record head via head drive network C35/C45/L5/R86 and record head relay K1. The head drive network provides a constant head current over a wide frequency range of the output of the record amplifier. Inductor L5 decouples resistor R86 so that the head inductance forms a resonant circuit with capacitor C45 at the bias frequency (432 kHz).

Record head relay K1 shunts the record winding of the head except during record mode. Relay driver R68/CR10/CR14/Q11, under control of the head relay control signal from the ramping amplifier in the control circuits, energizes record head relay K1 when the channel is not in the record mode. When the channel is not in the record mode, the head relay control signal from the control circuits is positive. The positive head relay control signal turns transistor Q11 on. With transistor Q11 conducting, relay K1 is energized and the normally-open contact of relay K1 is closed, providing a short across the record windings. When the channel goes into the record mode, the head relay control signal goes low and turns off transistor Q11, which de-energizes relay K1. When relay K1 is de-energized, the contacts across the record winding are opened and the short across the record winding is removed. When the short circuit across the record winding is removed, the output of the head drive network C35/C45/L5/R86 is supplied to the record winding high input. The return lead (low side) of the record winding returns to ground through a 10-ohm resistor R93. Test point TP9 of the high side of resistor R39 is provided to monitor the current through the record head winding.

4-75. Erase Circuit. The erase circuit provides filtering, buffering, and ramping of the 144-kHz erase signal from the master erase bus to the erase head. A simplified block diagram of the erase circuit is shown in Figure 4-21.

As shown in Figure 4-21, the erase circuitry receives 144-kHz from the master erase bus and the erase ramping control from the control logic. The SAFE/REC signal controls, via the erase ramping control amplifier on the control logic, the ramp on and ramp off of the erase signal to the erase amplifier and the erase head. During record mode, the 144-kHz signal goes through resistor R83 to erase ramping switch Q14 and filter C67/L6. Filter C67/L6 is a 144-kHz bandpass filter which removes the harmonics from the received 144-kHz signal.

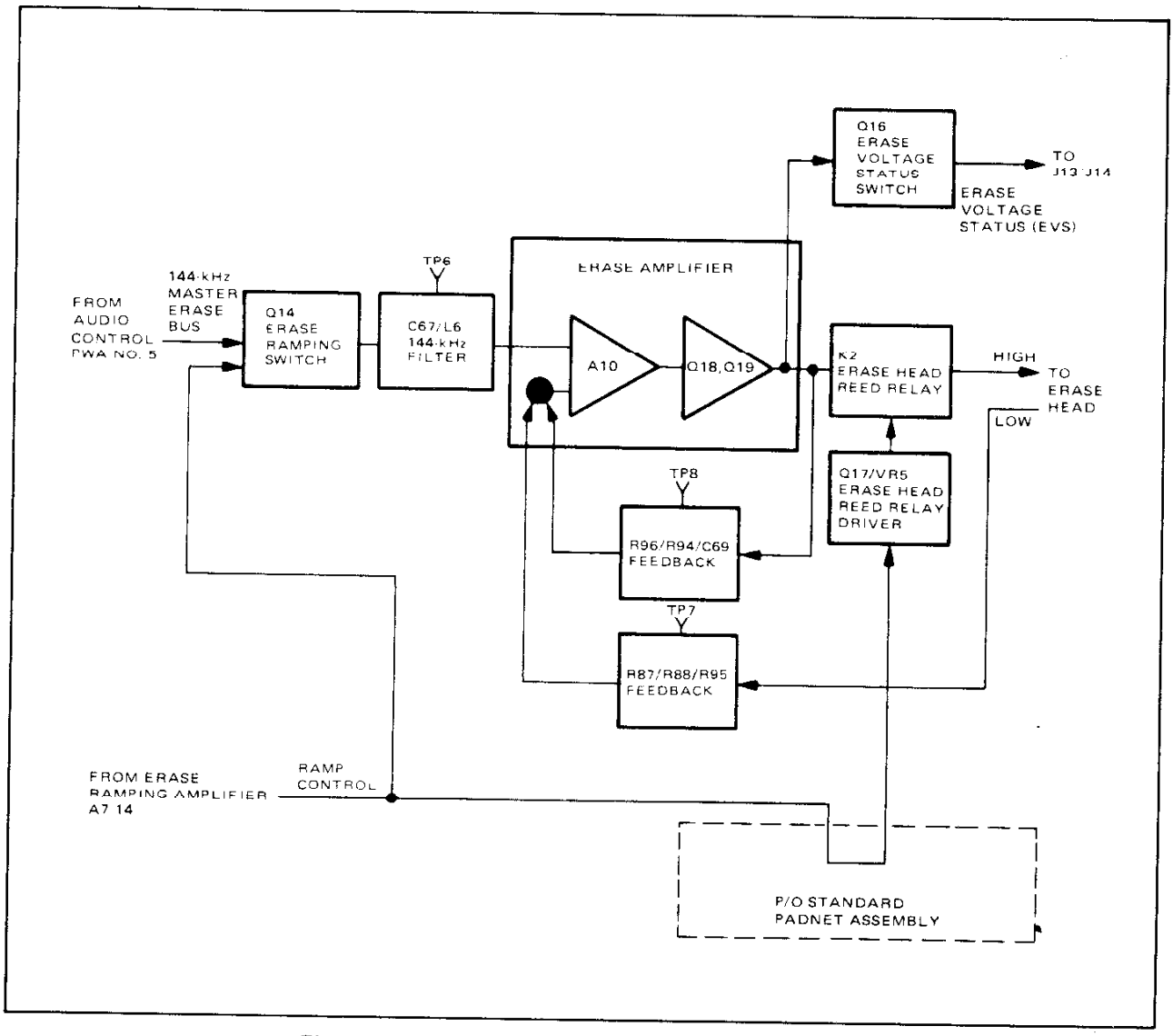


Figure 4-21. Erase Circuit, Simplified Block Diagram

Erase ramping switch Q14, operating in the inverted mode, acts as a shunt across filter C67/L6 which ramps the erase bias on and off. The filtered 144-kHz signal, when ramped on, goes to erase amplifier A10/Q18/Q19.

Erase amplifier A10/Q18/Q19 consists of amplifier A10 and complementary pair transistor driver amplifier Q18/Q19 arranged to form a feedback-controlled current driver to the erase head. The filtered 144-kHz signal is applied to the non-inverting input of amplifier A10. Feedback voltage from the output of driver amplifier Q18/Q19 via resistor R96 is summed with the current feedback developed across resistor R87 via resistor R88 at the inverting input of amplifier A10. The output 144-kHz erase signal from driver amplifier Q18/Q19 goes through capacitor C71 and contacts of reed relay K2 to the erase head. During record, reed relay K2 is energized by erase head relay

driver Q17/VR5. The output of the driver amplifier Q18/Q19 also goes to the erase voltage status switch Q16 which supplies a low to the erase voltage status line (EVS) when the erase voltage is present at the output of driver amplifier Q18/Q19.

When the channel is not in the record mode, the 144 kHz from the master erase bus through resistor R83 is shunted to ground by erase ramping switch Q14, and erase head relay K2 is de-energized, which opens the circuit to the winding of the erase head.

4-76. Reproduce Circuits. The reproduce circuits provide amplification, selection, and post-equalization of the playback signals. Figure 4-22 shows a simplified block diagram of the reproduce circuits.

As shown in Figure 4-22, the reproduce circuit contains the sel sync head preamplifier, reproduce head preamplifier, and reproduce equalizer amplifier. The reproduce head preamplifier receives the playback signal from the reproduce head and is located on the main audio PWA. The sel sync head preamplifier receives the playback signal from the sel sync winding on the record head and is also located on the audio main board. The outputs of the two head preamplifiers go to the standard PADNET assembly where, via the individual sel sync and reproduce gain controls, the signal is applied to the summing point at the input to the reproduce equalizer amplifier through the sel sync and reproduce switching FETs. The reproduce equalizer amplifier provides post-equalization of the selected playback signal. The output of the reproduce equalizer amplifier is fed back, via speed selected equalization and compensating networks located on the PADNET assembly, to the summing point at the input of the reproduce equalizer amplifier. The output of reproduce equalizer amplifier is also sent to the audio output amplifier via erase frequency trap C3/L1 and input resistors R8/R9.

The signal from the sel sync winding on the record head is connected through capacitor C31 to the input of the sel sync preamplifier. Sel sync winding shunt switch Q6 at the input to the sel sync preamplifier consists of transistor switch Q6, operating in the inverted mode which shorts out the sel sync winding during record. Transistor switch Q6 is controlled by the output of the bias ramping control amplifier A7-8 in the control logic. Resistor R33, in parallel with the input to the sel sync preamplifier, provides damping of the sel sync winding at resonance. The sel sync preamplifier consists of transistor Q5 and amplifier A4 arranged as a feedback-controlled voltage amplifier. The signal from the sel sync winding of the record head is fed to the base of transistor Q5. The output from transistor Q5 is fed to the inverting input of amplifier A4. Part of the output from amplifier A4 is fed back to the emitter of transistor Q5 via network C11/C12/C18/R12/R15-R17. The network formed by R15, R16, and C18 provides additional negative feedback to attenuate mid-range and high frequencies, thereby providing a low frequency boost in the output of sel sync preamplifier to compensate for the inherent roll-off in the reproduce signal from the sel sync windings. Resistor R17, in conjunction with C28/R37, sets the low-frequency gain of the sel sync head preamplifier. Capacitor C12 and inductor L2 in this network form a series-resonant trap at the bias frequency. The output of the sel sync head preamplifier A4, via resistor R49, goes to the unequalized sel sync output at the PWA-edge connector. From here the signal is routed to connector J13/J14. The output of the sel sync head preamplifier, via capacitor C13, goes to the sync gain control R3/R4 located on the PADNET assembly.

In a similar manner, the audio from the reproduce head is amplified by the reproduce head preamplifier consisting of operational amplifier A3 and transistor Q4 arranged to form a feedback controlled amplifier. The audio from the reproduce head goes to the base of transistor Q4 via inductor L3 which provides RFI filtering. Head damping network R36/R34, in parallel with the audio input to the base of transistor Q4, provides adjustable damping of the high-frequency head resonance. The output from amplifier A3 is fed back to the input of transistor Q4 via RC network C24/R31. This RC network, together with RC network C27/R32, sets the ac gain of the reproduce head preamplifier. Another RC network formed by R23/C23 limits the open loop gain of operational amplifier A3.

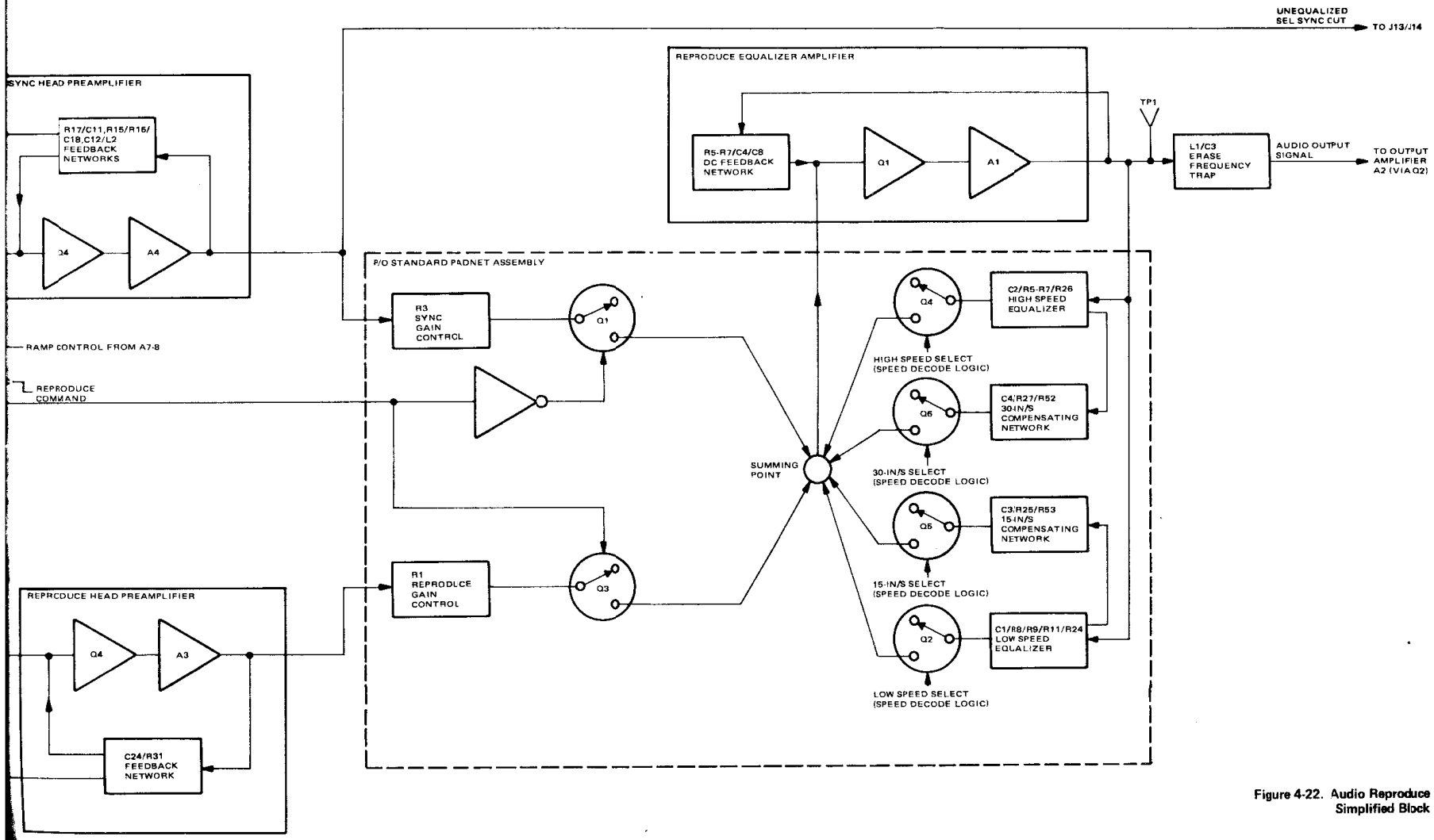
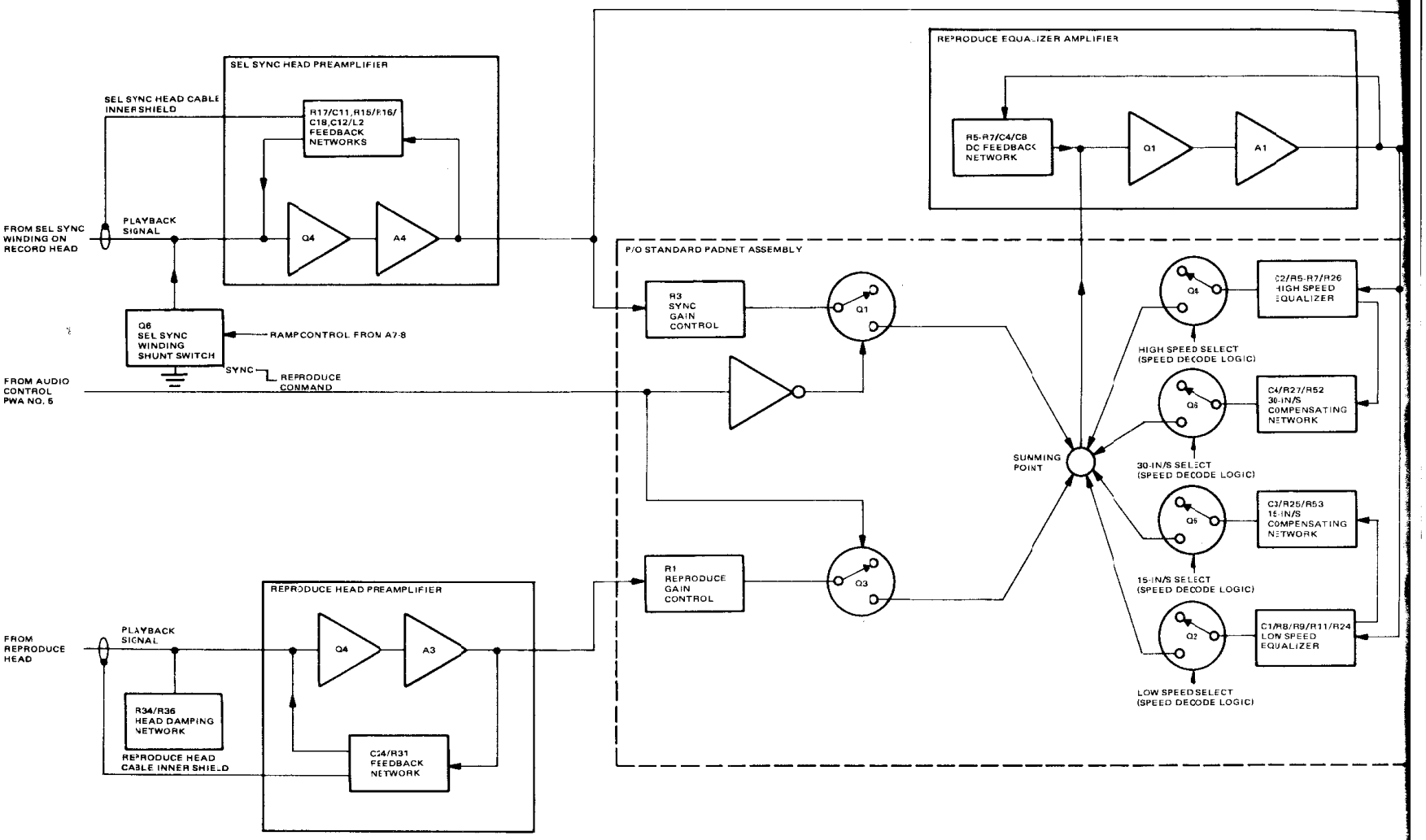


Figure 4-22. Audio Reproduce Circuits, Simplified Block Diagram



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The output of the reproduce head preamplifier, via capacitor C7, goes to the reproduce gain control R1 on the PADNET assembly. The PADNET assembly contains the switching for selecting the output of the sel sync head preamplifier or reproduce head preamplifier as the input to the reproduce equalizer amplifier. The PADNET assembly also contains the switching and equalizer networks which provide feedback to the reproduce equalizer amplifier for post-equalization of the reproduce audio. The SYNC/REPRO signal from the audio control assembly, via FET switches Q1 and Q3, selects the signal from either the sync gain control R3 or reproduce gain control R1 as the input to the reproduce equalizer amplifier. The selected playback signal goes to the summing point at the input to the reproduce equalizer amplifier.

The reproduce equalizer amplifier consists of a high gain, low-noise differential amplifier Q1, operational amplifier A1, and RC network R5-R7/C4/C6. The RC network provides dc feedback to the inverting input of amplifier Q1, which prevents dc output saturation in the event that power is applied with the PADNET not installed. The summing point at the input to amplifier Q1 also receives dc feedback via the selected equalizing network.

The reproduce equalization network contains two post-equalization networks, one for high speed and one for low speed. The high speed and low speed post-equalization feedback networks are selected by FET switch Q4 and FET switch Q2, respectively, which are gated by the decoded high- and low-speed selection signals from the speed decode logic. When 30- or 15-in/s speeds are selected, additional equalization is required to compensate for secondary gap effect which is more pronounced at these speeds.

The 30-in/s and 15-in/s signals from the speed decode logic enable additional equalization, via FET switches Q6 and Q5 respectively, to be inserted in parallel to the high- or low-speed equalizing feedback loop. The output from the reproduce equalizer amplifier is applied to the summing junction of the output amplifier via gain setting resistors R8 and R9 when the tape selection FET switch Q2 is in the tape mode. An LC network L1/C3, in conjunction with R8, forms a series-resonant trap at the erase frequency for the signal sent to FET switch Q2.

4-77. Audio Output Circuit. The audio output circuit consists of FET switches Q3 and Q2, audio output amplifier A2, and feedback network R11/C9. Figure 4-23 is a simplified block diagram of the audio output circuit. FET switches Q3 and Q2 provide selection of either tape or input signals to be buffered by audio output buffer A2 under control of the $\overline{\text{TAPE}}$/TAPE and $\overline{\text{INPUT}}$/INPUT command signals from the audio control PWA No. 5. FET switch Q2 selects the off-tape signal from the reproduce equalizer amplifier when the $\overline{\text{TAPE}}$/TAPE command goes low. For monitoring, FET switch Q3 selects the audio input signal to the record circuits when the $\overline{\text{INPUT}}$/INPUT signal goes low. FET switches Q2 and Q3 will never both be turned on at the same time; however, both switches may be turned off simultaneously. Diode CR1 at the input to FET switch Q2 provides limiting, when Q2 is turned off, of positive signal peaks to ensure that FET switch Q2 is not turned on by the signal peaks. When FET switch Q2 is turned on by the $\overline{\text{TAPE}}$/TAPE signal, diode CR1 will not be forward biased because diode CR1 is essentially at the virtual ground of the summing junction. In a similar manner, diodes CR2 and CR20 at the input of FET switch Q3 provide a symmetrical clamp for the audio input to the switch which prevents the audio peaks from turning on FET switch Q3.

The selected audio, either tape or input, goes to the inverting input of audio output buffer A2 which provides, via resistor R12, the audio output signal from the main audio PWA. Part of the audio output signal is fed back to the input of audio output buffer A2 by feedback network R11/C9. The voltage feedback from this network, together with resistors R22 or R8/R9 selected by FET switches Q3 or Q2, set the required closed loop gain of audio output buffer A2.

4-78. Input/Output Assembly (Accessory)

Up to two input/output modules may be mounted side-by-side in an input/output assembly. One module is required for each audio channel, and each module contains a line input and a line output

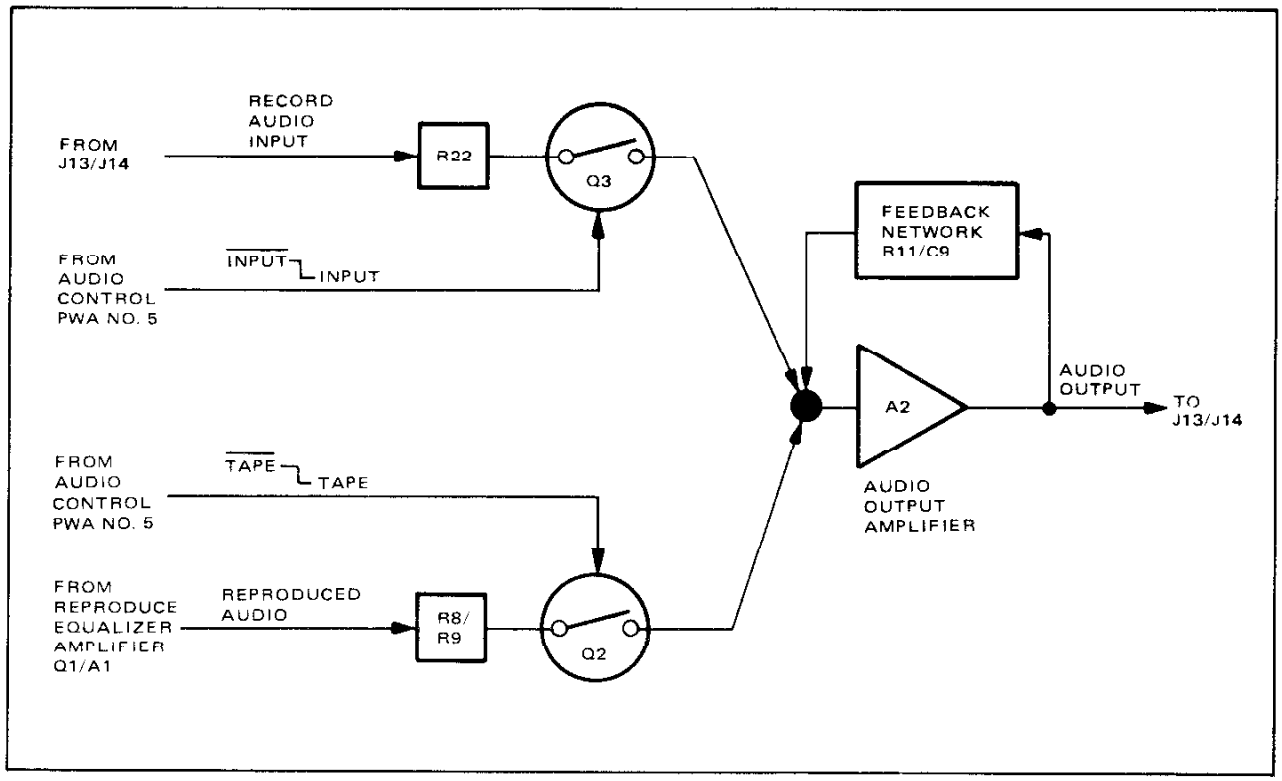

Figure 4-23. Audio Output Circuit, Simplified Block Diagram

transformer that permits balanced line operation, a line driver, switchable peak/vu level meter, and input and output level controls with preset/manual switch controls. Figure 4-24 is a simplified block diagram of the input/output assembly, drawing 4840427 is the schematic of the input/output mainframe assembly, and drawing 4840421 is the schematic of the input/output module (schematics are in Section 6 of this manual).

4-79. Line Input Amplifier. The audio line input signal to be recorded is applied to the input of the input/output assembly. This signal can be either balanced or unbalanced (see Installation section), and the signal is fed through input transformer T2 to RECORD MANUAL/PRESET switch S2. In the PRESET position, the gain of line input operational amplifier is adjusted by record preset potentiometer R2 to provide a −5-dBm output level to the ATR-100 when the input is +4 dBm (or other input level as selected by the user).

If other than a predetermined input line level is fed to the input, switch S2 is placed in the MANUAL position and the RECORD potentiometer control is used to control the gain of the amplifier A2 to provide a −5 dBm output operating level to the ATR-100. If required, the gain of amplifier A2 may be increased +6 dB by installing a jumper across series resistors R60 and R63 and changing C20 to 47 pF. (This also changes the input impedance from 50K to 25K ohms.) Offset null control R55 is adjusted so there is zero change in dc voltage when the RECORD potentiometer control is rotated through its range.

4-80. Input Signal Monitoring. In input monitoring mode, the line input signal can be monitored on the level meter and on the line-output line. The line input is sampled at the output of amplifier A2 and is fed through record calibrate potentiometer R3 to the input of FET switch Q2. In input monitoring mode, the $\overline{\text{tape}}$/tape command from the

ATR-100 is high ($\overline{\text{tape}}$). This high turns FET switch Q1 off and the high is inverted by Q3. The low from the collector of Q3 turns FET switch Q2 on and the line input signal is fed to the line output amplifier. The output amplifier is formed from operational amplifier A5-6 and complementary symmetry line-driver transistors Q4 and Q5 which feed line output transformer T1. The gain of the output amplifier is set by two feedback loops. The first feedback loop is from the output of Q4/Q5 via R23/C6; and the second feedback loop is derived from a tertiary winding on output transformer T1, which supplies approximately 8 dB of additional feedback, via R22/C5 to the summing node of A5-2. The output signal can be either balanced or unbalanced (see Installation section of manual).

Record calibrate potentiometer R3 is adjusted so that the −5-dBm level at the output of amplifier A2 is amplified to provide a +4-dBm line-output level (or other output level as selected by the user). Offset null control R40 is adjusted so there is zero volts at TP2 when no input signal is applied to the input/output assembly.

4-81. Reproduce Mode. In reproduce mode, the reproduced audio signal at a −5-dBm level from the ATR-100 is applied to the REPRODUCE control and the reproduce preset control R1. Control R1 is adjusted so that when REPRODUCE switch S1 is in the PRESET position, the output line level will be +4 dBm (or other output level as selected by the user). For manual adjustment of output line level, switch S1 is placed in the MANUAL position and the REPRODUCE potentiometer control is adjusted for the desired line-output level. In reproduce mode, the $\overline{\text{tape}}$/tape command from the ATR-100 is low (tape). This low enables FET switch Q1 and, via inverter Q3, disables FET switch Q2. When Q1 is enabled, the audio signal from the ATR-100 is applied to the input of operational amplifier A5.

4-82. Meter Circuit Operation. The signal to be displayed on the meter is sampled from the tertiary feedback winding on output transformer T1. This signal is applied to meter calibration potentiometer control R21, which is set so that a +4-dBm line output signal (or other level selected by the user) will indicate 0 vu on the level meter when the peak/vu switch S3 is in the vu position. (In the peak position the meter will read −6 when R21 has been set to read 0 vu in vu position.) The signal at the wiper of R21 is applied to the non-inverting input of operational amplifier A4. This amplifier has its output connected to the full-wave bridge rectifier formed by CR3-CR6. Current feedback from the lower side of the bridge (junction of CR5/CR6) is applied to the inverting input of A4-6. This feedback linearizes the diode transfer characteristics to produce a precision full-wave rectifier. Components R19/C9/C10 set the ac gain of the circuit in conjunction with resistor R30.

The rectified output of the diode bridge appears across R30 and is applied to the differential inputs of A1-1. The output of A1-1 is a full-wave rectified signal referred to ground level. This signal is fed to amplifier A3-1, which uses Q6 as an output current amplifier. Amplifier A3-1 and Q6 provide a high drive current stage which is required when charging the peak mode holding capacitor C1. Time constant components C1/R24 determine peak mode integration time and time constant components C1/R4 predominately determine the fallback time.

In peak mode, switch S3A connects the input and feedback network R5/R12/R13/C3 around meter drive amplifier A1-7. In vu mode, switch S3B disconnects the integration capacitor C1, and switch S3A connects the other input/feedback network R10/R11/C2 and R9/C4 around meter drive amplifier A1-7. These switched networks provide the necessary gain change for peak and vu metering in addition to providing the correct meter ballistic for both modes.

Offset null control R32 is adjusted so that the level meter will show no deflection (same reading as when power is removed and meter needle is at extreme left-hand dial position) when no signal is applied to the input/output assembly.

4-83. Erase and Bias Voltage Confidence Indicators. The ERASE and BIAS LED indicators illuminate when the ATR-100 is in the record mode. In record mode, the EVS (erase voltage status) and BVS (bias voltage status) commands are low. These commands cause Q9 and Q10 to conduct, which causes the LED indicators to illuminate.

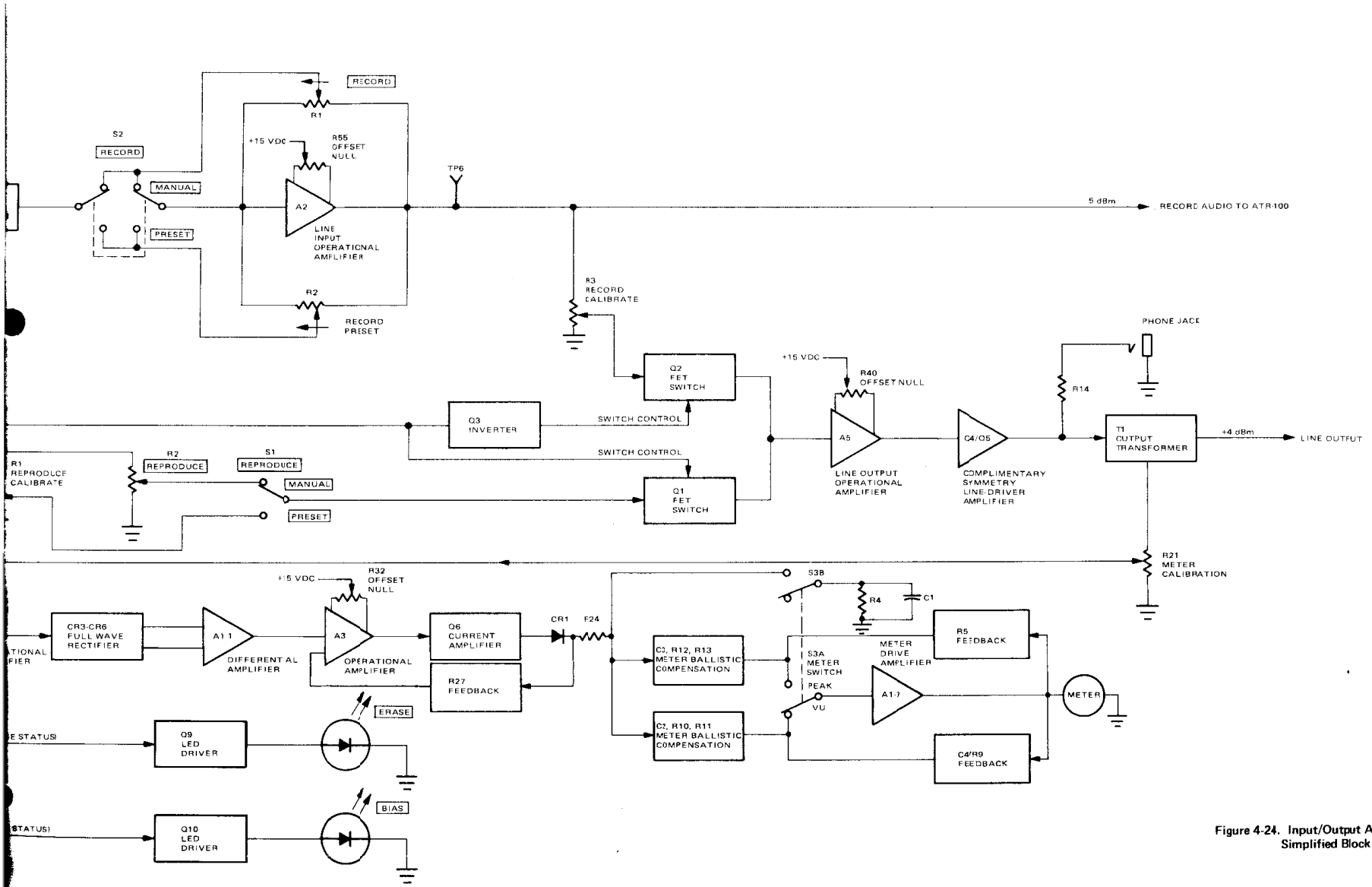

Figure 4-24. Input/Output Assembly, Simplified Block Diagram